# Heating of semiconductor devices in electric circuits

Markus Brunk and Ansgar Jüngel

**Abstract** Thermal effects in a coupled circuit-device system are modeled and numerically simulated. The circuit equations arise from modified nodal analysis. The transport in the semiconductor devices is modeled by the energy-transport equations for the electrons and the drift-diffusion equations for the holes, coupled to the Poisson equation for the electric potential. The lattice temperature is described by a heat equation with a heat source including energy relaxation heat, recombination heat, hole Joule heating, and radiation. The circuit-device model is coupled to a thermal network. The resulting system of nonlinear partial differential-algebraic equations is discretized in time using backward difference formulas and in space using (mixed) finite elements. Heating effects from numerical simulations in a *pn*-junction diode and a clipper circuit are presented.

## 1 Introduction

In modern ultra-integrated computer chips, secondary effects like self-heating are strongly influencing the switching behavior of the transistors and the performance of the circuit. In order to control the thermal effects, accurate circuit simulations are needed, which go beyond compact modeling and simplified temperature models. In this paper, we review a coupled circuit-device model taking into account the temperature of the electrons and the semiconductor lattice and the temperature of the circuit elements and present new numerical simulations illustrating the self-heating.

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First coupled circuit-device models were often based on a combination of device and circuit simulators [10]. More recently, electric network models were coupled to semiconductor transport equations, using drift-diffusion [14,16] or energy-transport models [8]. Nonisothermal device modeling started in the 1970s, employing drift-diffusion-type equations and heat flow models for the lattice temperature [1]. A thermodynamic approach to extend the drift-diffusion equations to the nonisothermal case was presented in [17], later generalized in [2] using first principles of entropy maximization and partial local equilibrium. In [3], the energy-transport equations were coupled to a heat equation for the lattice temperature.

All these references are concerned with the modeling of certain subsystems. Here, based on our work [9], we present a complete coupled model, including (i) the device model consisting of the energy-transport equations for the electrons, the drift-diffusion equations for the holes, and a heat equation for the lattice temperature, (ii) the electric-network equations, and (iii) a thermal network model describing the heat evolution in the circuit elements, electric lines, and devices. The models are described in Section 2. The three subsystems are coupled by thermo-electric, electric circuit-device, and thermal network-device interfaces explained in Section 3. Finally, in Section 4, the heating behavior in a *pn*-junction diode and a clipper circuit is illustrated.

## 2 Model Equations

**Device modeling.** The electron transport in the semiconductor device is modeled by the energy-transport equations, whereas the hole transport is described by the drift-diffusion equations. The equations for the electron density $n$, the electron thermal energy $\frac{3}{2}k_BnT_n$ (with $k_B$ being the Boltzmann constant), the hole density $p$, and the self-consistent electric potential $V$ read as

$$\partial_t n - q^{-1}\operatorname{div} J_n = -R(n,p), \quad \partial_t p + q^{-1}\operatorname{div} J_p = -R(n,p), \tag{1}$$

$$\partial_t(\tfrac{3}{2}k_BnT_n) - \operatorname{div} J_w + J_n\cdot\nabla V = W(n,T_n) - \tfrac{3}{2}k_BT_nR(n,p), \tag{2}$$

$$\varepsilon_s\Delta V = q(n-p-C(x)), \tag{3}$$

where $q$ is the elementary charge, $\varepsilon_s$ the semiconductor permittivity, and $C(x)$ the doping concentration. The function $R(n,p)$ models Shockley-Read-Hall recombination-generation processes and $W(n,T_n)$ describes the relaxation to the lattice temperature $T_L$,

$$R(n,p) = \frac{np-n_i^2}{\tau_p(n+n_i)+\tau_n(p+n_i)}, \quad W(n,T_n) = \frac{3}{2}\frac{nk_B(T_L-T_n)}{\tau_0}, \tag{4}$$

where $n_i$ is the intrinsic density, $\tau_n$ and $\tau_p$ the electron and hole lifetimes, respectively, and $\tau_0$ the energy relaxation time.

The constitutive relations for the electron current density $J_n$, the hole current density $J_p$, and the electron energy density $J_w$ are given by

$$J_n = q\Big(\nabla\Big(\mu_n\frac{k_BT_L}{q}n\Big) - \mu_nT_L\frac{n}{T_n}\nabla V\Big), \quad J_p = -q\Big(\nabla\Big(\mu_p\frac{k_BT_L}{q}p\Big) + \mu_pp\nabla V\Big), \tag{5}$$

$$J_w = \nabla\Big(\frac{3}{2}\mu_nT_n\frac{k_B^2T_L}{q}n\Big) - \frac{3}{2}\mu_nk_BT_Ln\nabla V, \tag{6}$$

where the mobilities for the electrons and holes, $\mu_n$ and $\mu_p$, respectively, are assumed to depend on the lattice temperature $T_L$ according to

$$\mu_j(T_L) = \mu_{j,0}\Big(\frac{T_0}{T_L}\Big)^{\alpha_j}, \quad j = n,p, \tag{7}$$

where $T_0 = 300\,\mathrm{K}$. The values $\mu_{j,0}$ and $\alpha_j$ ($j = n,p$) are typically determined from measurements; see, for instance, [13, Table 4.1-1]. The energy-transport equations were derived from the semiconductor Boltzmann equation by a moment method assuming dominant elastic scattering [7, 11].

The total semiconductor current density $J_{\mathrm{tot}} = J_n + J_p + J_d$ is the sum of the particle current densities and the displacement current density $J_d = -\varepsilon_s\partial_t\nabla V$. The current leaving the semiconductor device, which occupies the domain $\Omega \subset \mathbb{R}^d$ ($d \geq 1$), at terminal $\Gamma_k$ is defined by

$$j_k = \int_{\Gamma_k} J_{\mathrm{tot}}\cdot\nu ds, \tag{8}$$

where $\nu$ is the exterior normal unit vector to $\Gamma_k$. Due to charge conservation, the current through one terminal can be computed by the negative sum of the other terminal currents. We choose one terminal as the reference terminal and denote by $j_S$ the vector of all terminal currents except the reference terminal.

The model equation for the lattice temperature is derived from thermodynamic principles. Assuming that the thermal effects are due to the majority carriers (electrons), the free energy for the system of energy-transport and Poisson equations is the sum of the electric energy, the thermodynamic energy of the lattice subsystem, and the thermodynamic energy of the electron subsystem [2, 5],

$$f = \frac{\varepsilon_s}{2}|\nabla V|^2 + \rho_Lc_LT_L(1-\log T_L) + n\Big[k_BT_n\Big(\log\frac{n}{N_c} - 1\Big) + E_c\Big],$$

where $\rho_L$ denotes the material density, $c_L$ the heat capacity, $E_c$ the conduction-band energy, and $N_c = 2(m_e^*k_BT_n/2\pi\hbar^2)^{3/2}$ the effective density of states, with the effective electron mass $m_e^*$ and the reduced Planck constant $\hbar = h/2\pi$. Then, the internal total energy is given by

$$u = f - T_n\frac{\partial f}{\partial T_n} - T_L\frac{\partial f}{\partial T_L} = \frac{\varepsilon_s}{2}|\nabla V|^2 + \rho_Lc_LT_L + n(E_c - T_LE_c') + \frac{3}{2}k_BnT_n,$$

where the prime denotes the derivative with respect to $T_L$. The associated total energy flux density $J_u$ is the sum of the energy flux in the electric field, the Fourier heat flux, and the electron energy flux:

$$J_u = VJ_{\text{tot}} - \kappa_L \nabla T_L - (E_c - T_L E_c')q^{-1}J_n - J_w,$$

where $\kappa_L$ is the heat conductivity of the lattice. Inserting the expressions for the total internal energy and its flux into the energy balance equation $\partial_t u + \operatorname{div} J_u = -\gamma$, where $\gamma$ models the radiation, and employing the Poisson equation for $\partial_t V$, a straightforward computation leads to the heat equation for the lattice temperature (see [9] for details):

$$0 = \partial_t u + \operatorname{div} J_u + \gamma = \partial_t T_L(\rho_L c_L - nE_c') - \operatorname{div}(\kappa_L \nabla T_L) - H, \tag{9}$$

where $\gamma = S_L(T_L - T_{\text{env}})$ is the energy loss by radiation with the transmission constant $S_L$ and the environmental temperature $T_{\text{env}}$, and $H$ is the heat source term,

$$H = -W + R\big(E_c - T_L E_c' + \tfrac{3}{2}k_B T_n\big) + q^{-1}J_n \cdot \nabla(E_c - T_L E_c') - J_p \cdot \nabla V - S_L(T_L - T_{\text{env}}),$$

where the relaxation term $W$ is defined in (4). For related but different choices of the heat source term, we refer to the discussion in [17]. For nondegenerate homostructure devices, we can neglect the space dependency of the energy band. Furthermore, we neglect the dependency of the energy band on the lattice temperature since this dependency is rather small [13]. Thus, the heat source term becomes

$$H = -W + R\big(E_c + \tfrac{3}{2}k_B T_n\big) - J_p \cdot \nabla V - S_L(T_L - T_{\text{env}}),$$

The first term in $H$ represents the energy relaxation heat, the second term is the recombination heat, the third term expresses Joule heating from the holes, and the last term signifies the radiation.

The model equations (1)-(9) are complemented by initial and boundary conditions. The boundary $\partial\Omega$ of the semiconductor domain is assumed to consist of the union of Ohmic contacts $\Gamma_C = \cup_k \Gamma_k$ and the union of insulating boundary segments $\Gamma_I$ such that $\Gamma_C \cup \Gamma_I = \partial\Omega$ and $\Gamma_C \cap \Gamma_I = \emptyset$. We prescribe initial conditions for the electron density $n$, the electron temperature $T_n$, and the lattice temperature $T_L$ in $\Omega$.

On the insulating boundary parts, the normal components of the current densities, the electric field and the temperature flux are assumed to vanish,

$$J_n \cdot \nu = J_p \cdot \nu = J_w \cdot \nu = \nabla V \cdot \nu = \nabla T_L \cdot \nu = 0 \quad \text{on } \Gamma_I,\ t > 0. \tag{10}$$

The electric potential at the contacts is the sum of the applied voltage $V_{\text{app}}$ and the built-in potential $V_{\text{bi}}$,

$$V = V_{\text{app}} + V_{\text{bi}} \quad \text{on } \Gamma_C,\ t > 0, \quad \text{where} \quad V_{\text{bi}} = \operatorname{arsinh}(C(x)/2n_i). \tag{11}$$

According to the numerical results of [4], we may suppose that the normal component of the electron temperature vanishes on $\Gamma_C$. In order to model the temperature

exchange between the semiconductor device and the sourrounding network with the temperature $T_{\rm env}$, we employ a Robin boundary condition for the lattice temperature:

$$\nabla T_n \cdot \nu = 0, \quad -\kappa_L \nabla T_L \cdot \nu = R_{\rm th}^{-1}(T_L - T_{\rm env}) \quad \text{on } \Gamma_C,\ t > 0, \tag{12}$$

where $R_{\rm th}$ is the thermal resistivity of the contact. For the particle densities, we use, as motivated in [8], the Robin conditions

$$n + (\theta_n \mu_n)^{-1} J_n \cdot \nu = n_a, \quad p - (\theta_p \mu_p)^{-1} J_p \cdot \nu = p_a \quad \text{on } \Gamma_C,\ t > 0, \tag{13}$$

where $(n_a, p_a)$ is the solution of the charge-neutrality equation $n_a - p_a - C(x) = 0$ and the thermal equilibrium condition $n_a p_a = n_i^2$, and $\theta_n$, $\theta_p$ are some positive parameters ($\theta_n = \theta_p = 2500$ in the simulations; see [8]).

**Circuit modeling.** The electric circuit is assumed to contain only (ideal) resistors, capacitors, inductors and voltage and current sources. To simplify the presentation, the circuit only contains one semiconductor device. The circuit is modeled by employing modified nodal analysis [16], whose basic tools are the Kirchhoff current and voltage laws and the current-voltage characteristics of the basic elements. We replace the circuit by a directed graph with branches and nodes. Branch currents, branch voltages, and node potentials (without the mass node) are introduced as (time-dependent) variables. Then, the circuit can be characterized by the incidence matrix $A = (a_{ik})$ describing the node-to-branch relations,

$$a_{ik} = \begin{cases} 1 & \text{if the branch } k \text{ leaves the node } i, \\ -1 & \text{if the branch } k \text{ enters the node } i, \\ 0 & \text{else.} \end{cases}$$

The network is numbered in such a way that the indidence matrix consists of the block matrices $A_R$, $A_C$, $A_L$, $A_i$, and $A_v$, where the index indicates the resistive, capacitive, inductive, current source, and voltage source branches, respectively. The semiconductor device is included into the network model employing the semiconductor indicence matrix $A_S = (a_{ik}^S)$ defined by

$$a_{ik}^S = \begin{cases} 1 & \text{if the current } j_k \text{ enters the circuit node } i, \\ -1 & \text{if the reference terminal is connected to the node } i, \\ 0 & \text{else.} \end{cases}$$

The current-voltage characteristics for the basic elements are given by

$$i_R = g_R(v_R), \quad i_C = \frac{dq_C}{dt}(v_C), \quad v_L = \frac{d\phi_L}{dt}(i_L),$$

where $g_R$ denotes the conductivity of the resistor, $q_C$ the charge of the capacitor, and $\phi_L$ the flux of the inductor. Moreover, $i_\alpha$ and $v_\alpha$ with $\alpha = R, C, L$, are the branch current vectors and branch voltage vectors for, respectively, all resistors, capacitors, and inductors.

Denoting by $i_s = i_s(t)$, $v_s = v_s(t)$ the input functions for the current and voltage sources, respectively, the Kirchhoff laws lead to the following system of differential-algebraic equations in the charge-oriented modified nodal approach [16]:

$$A_C \frac{dq_C}{dt}(A_C^\top e) + A_R g_R(A_R^\top e) + A_L i_L + A_v i_v + A_S j_S = -A_i i_s, \tag{14}$$

$$\frac{d\phi_L}{dt}(i_L) - A_L^\top e = 0, \quad A_v^\top e = v_s, \tag{15}$$

for the unknowns $e(t)$, $i_L(t)$, and $i_v(t)$, where $e(t)$ denotes the vector containing the node potential and $j_S$ is the vector of all terminal currents defined in (8). The circuit is coupled to the device through the semiconductor current $j_S$ in (14) and through the boundary conditions for the electric potential. At terminal $\Gamma_k$, it holds $V(t) = e_i(t) + V_{\rm bi}$ if the terminal $\Gamma_k$ is connected to the circuit node $i$.

Equations (14)-(15) represent a system of differential-algebraic equations. Under certain assumptions on the topology of the network, it was shown that the (tractability) index of the system is at most two [15, 16]. Furthermore, if the circuit does neither contain so-called LI-cutsets nor CV-loops with at least one voltage source, the index is at most one.

**Thermal network modeling.** The thermal network consists of lumped thermal elements, i.e. zero-dimensionally modeled elements with temperature value $\widehat{T}^\ell(t)$; distributed thermal lines, i.e. spatially one-dimensional elements with temperature $T^d(x,t)$; and distributed semiconductor devices with the lattice temperature $T_L(x,t)$ as described above. Adjacent lumped elements are considered as a zero-dimensional unit with temperature $\widehat{T}$. We assign the temperature at the interface of connected distributed elements to an artificial zero-dimensional element (thermal node) with temperature $\widehat{T}$ and without thermal mass. This forms a network with lumped-distributed interfaces only, in which the nodes represent the zero-dimensional units and the branches represent the distributed elements.

The thermal network is characterized by the thermal incidence matrix $A_d^{\rm th} = (a_{ij}^{\rm th})$ and the thermal semiconductor incidence matrix $A_S^{\rm th} = (a_{S,ij}^{\rm th})$ defined by

$$a_{ij}^{\rm th} = \begin{cases} 1 & \text{if the contact at } x = 0 \text{ of branch } j \text{ is connected to node } i, \\ 1 & \text{if the contact at } x = L_{\rm th} \text{ of branch } j - m_d \text{ is connected to node } i, \\ 0 & \text{else,} \end{cases}$$

$$a_{S,ij}^{\rm th} = \begin{cases} 1 & \text{if the terminal } j \text{ is connected to thermal node } i, \\ 0 & \text{else,} \end{cases}$$

where $m_d$ is the number of thermal lines and $[0, L_{\rm th}]$ the interval of the distributed element.

The temperature in the thermal nodes evolves according to the heat equation

$$\widehat{\mathbf{M}} \frac{d\widehat{\mathbf{T}}}{dt} = \widehat{\mathbf{F}}^d + \widehat{\mathbf{F}}^S - \widehat{\mathbf{S}}(\widehat{\mathbf{T}} - T_{\rm env}\mathbf{I}) + \widehat{\mathbf{P}}, \quad t > 0. \tag{16}$$

Here, $\widehat{\mathbf{M}}$ is a diagonal matrix containing the thermal masses of the thermal nodes, each of which is given as the sum of the thermal masses of the lumped elements contributing to the corresponding node. The thermal mass is the product of the heat capacity, the material density, and the physical volume of the corresponding element. Furthermore, $\widehat{\mathbf{T}}$ is the vector of all temperature values in the thermal nodes, and $\mathbf{I}$ is the identity matrix. The electro-thermal source vector for the thermal nodes $\widehat{\mathbf{P}}$ and the heat flux vectors from the distributed lines $\widehat{\mathbf{F}}^d$ and the device $\widehat{\mathbf{F}}^S$ are defined below in (20), (18), and (19), respectively. The temperature values in the lumped elements $\widehat{\mathbf{T}}^\ell$ can be computed from $\widehat{\mathbf{T}}$ by the formula $\widehat{\mathbf{T}} = M\widehat{\mathbf{T}}^\ell$, where the matrix $M = (m_{ij})$ relates the lumped elements to the thermal nodes, with $m_{ij} = 1$ if the lumped element $j$ belongs to the thermal node $i$ and $m_{ij} = 0$ else.

The vector $\mathbf{T}^d = (T_j^d)$ of all temperatures of the thermal lines satisfies

$$M_j \partial_t T_j^d = \partial_x(\kappa_j \partial_x T_j^d) - S_j(T_j^d - T_{\mathrm{env}}) + P_j, \quad x \in (0, L_j),\ t > 0, \tag{17}$$

where $M_j$ denotes the thermal mass of the $j$-th element of length $L_j$, $\kappa_j$ is the thermal conductivity, $S_j$ the transmission function, and $\mathbf{P} = (P_j)$ the electro-thermal source vector defined in (20). The above equation is complemented by initial conditions and Dirichlet boundary conditions, collected in the vectors $\mathbf{T}_0^d$ and $\mathbf{T}_1^d$.

## 3 Coupling Conditions

The heat equations (16) and (17) are coupled through the boundary conditions, $(\mathbf{T}_0^d, \mathbf{T}_1^d)^\top = (A_d^{\mathrm{th}})^\top \widehat{\mathbf{T}}$, and the following equation for the thermal flux:

$$\widehat{\mathbf{F}}^d = A_d^{\mathrm{th}} \begin{pmatrix} \Lambda_0 \partial_x \mathbf{T}^d(0,t) \\ -\Lambda_1 \partial_x \mathbf{T}^d(L_{\mathrm{th}},t) \end{pmatrix}, \tag{18}$$

where $L_{\mathrm{th}}$ denotes the length of a thermal line and $\Lambda_0$, $\Lambda_1$ contain the products of thermal conductivities and the cross sections of the thermal lines at the contacts at $x = 0$ and $X = L_{\mathrm{th}}$, respectively.

Next, we describe the coupling between the thermal network and the device. The influence of the network on the device is modeled by the last boundary condition in (12) on $\Gamma_k$, with $T_{\mathrm{env}}$ replaced by the temperature of the connected elements, $\mathbf{T}_a = (A_S^{\mathrm{th}})^\top \widehat{\mathbf{T}}$. The semiconductor heat flux at terminal $k$ is given by the integral

$$F_k^S = \int_{\Gamma_k} J_{\mathrm{th}}^S \cdot \nu \, d\sigma, \quad \text{such that} \quad \widehat{\mathbf{F}}^S(t) = A_S^{\mathrm{th}}(F_j(t))_j, \quad t > 0. \tag{19}$$

The thermal flux density $J_{\mathrm{th}}^S$ is derived by making the quasi-stationary assumption $\operatorname{div} J_u = 0$. Then, inserting the stationary balance equation for the electric energy, a computation shows that (see [9] for details)

$$\operatorname{div} J_{\mathrm{th}}^S + \nabla V \cdot (J_n + J_p) = 0, \quad \text{where} \quad J_{\mathrm{th}}^S = -\kappa_L \nabla T_L - q^{-1} E_c J_n - J_w.$$

This equation indicates that the flux $J_{\rm th}^{\rm S}$ is responsible for the heat production caused by the dissipated power and is therefore considered as a heat flux.

For the coupling between the electric and thermal network, we assume that only semiconductor devices and resistors are thermally relevant. Electric-to-thermal coupling occurs through the power dissipated by a resistor. We assume as in [6, Sec. 5.3] that the resistance is given by $R = 1 + \alpha_1 T_R + \alpha_2 T_R^2$, where $\alpha_1$ and $\alpha_2$ are some nonnegative parameters and $T_R$ is the temperature of the resistor. The vector $\mathbf{T}_R$ of all resistor temperature values can be determined from the temperature vectors of the thermal nodes $\widehat{\mathbf{T}}$ and of the distributed lines $\mathbf{T}^d$ by

$$\mathbf{T}_R = \widehat{K}^\top \widehat{\mathbf{T}} + K^\top \widetilde{\mathbf{T}}^d,$$

where the lumped values $\widetilde{\mathbf{T}}^d$ are computed from the distributed values $\mathbf{T}^d$ by taking the mean value, and the matrices $K = (k_{\ell j})$ and $\widehat{K} = (\widehat{k}_{\ell j})$ are defined by

$$k_{\ell j} = \begin{cases} 1 & \text{if the resistor } j \text{ corresponds to the thermal branch } \ell, \\ 0 & \text{else,} \end{cases}$$

$$\widehat{k}_{\ell j} = \begin{cases} 1 & \text{if the resistor } j \text{ corresponds to the thermal node } \ell, \\ 0 & \text{else.} \end{cases}$$

The electric-to-thermal coupling is realized by the source terms $\mathbf{P} = (P_j)$ and $\widehat{\mathbf{P}}$ in the heat equations (16) and (17):

$$\widehat{\mathbf{P}} = \widehat{K} P_R, \quad \mathbf{P} = L_R^{-1} K P_R, \quad \text{where } P_R = \operatorname{diag}(i_R) A_R^\top e, \tag{20}$$

$i_R$ contains the currents through all resistors, $A_R$ denotes the resistor incidence matrix, $e$ is the vector containing the node potentials, and $L_R$ is the resistor length. For a discussion about the proper choice of the local power distribution, we refer to [6].

## 4 Numerical examples

The complete coupled system for the electric and thermal network and the semiconductor devices consists of nonlinear partial differential-algebraic equations. In the following, we restrict ourselves to one-dimensional device models. The equations are discretized in time by backward difference formulas (BDF-1 or BDF-2) to pay tribute to the differential-algebraic character of the system. The heat equations and the Poisson equation are discretized in space by linear finite elements. The transport equations are discretized by an exponentially fitted mixed finite-element method using Marini-Pietra elements [12]. It is shown in [12] that, for the stationary model, this method guarantees current conservation and positivity of the discrete particle densities. These properties also hold for the BDF-1 time-discrete system and, under a step size restriction, for the BDF-2 time-discrete system. In the following simulations, the positivity of the discrete particle densities has always been obtained. The

nonlinear discrete system is iterated by a combination of a fixed-point strategy and a variant of the Gummel method; see [9] for details.

**Bipolar junction diode.** We illustrate first the lattice heating in a 100 nm silicon *pn* diode consisting of a 50 nm *p*-doped part with doping $-C_0 = -5 \cdot 10^{23}\,\mathrm{m}^{-3}$ and a 50 nm *n*-doped part with doping $C_0$. Initially, the device is assumed to be in thermal equilibrium. The same physical parameters as in [9] are employed. We apply a forward bias of 1.5 V to the diode. The transient response of the electron and lattice temperature is illustrated in Figure 1. The electron temperature increases quickly in the entire device with a temperature maximum of about 3300 K in the *n*-region and then decreases slightly until the steady state is reached with a temperature minimum around the junction. The increase of the lattice temperature is significantly slower with a maximum of 325 K at steady state. Due to the high thermal conductivity, the lattice temperature is almost constant in the device.

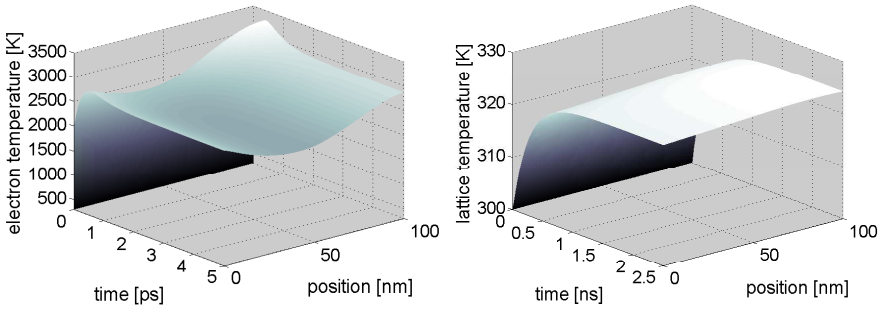


**Fig. 1** Transient electron temperature (left) and lattice temperature (right) in a *pn* diode at 1.5 V.

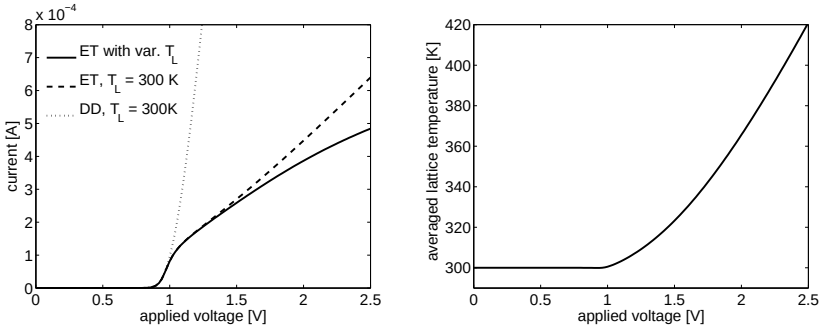


**Fig. 2** Left: Current-voltage characteristics of a *pn* diode computed from different models. Right: Averaged lattice temperature in a *pn* diode (stationary computations).

The influence of the lattice heating on the electrical performance of the device is shown in Figure 2. In the left figure, we compare the results computed from the

drift-diffusion (DD) model (using low-field mobilities) with those from the energy-transport (ET) equations with and without lattice heating. We observe that the current from the nonisothermal ET model is smaller than that from the ET model with constant lattice temperature. The right figure shows the averaged lattice temperature as a function of the applied voltage. For high applied bias, the lattice temperature reaches up to 420 K. However, we notice that a bias of 2.5 V might be unrealistic for the considered device.

**Clipper circuit.** A clipper is employed as an entrance protective circuit to avoid voltage peaks. It consists of two *pn* diodes (with the same parameters as in the previous example), one resistor with resistivity $R = 5\,\mathrm{k}\Omega$, and three voltage sources (see Figure 3). Here, $V_{\mathrm{in}}(t) = 5\sin(2\pi 10^{10}\,\mathrm{Hz}\,t)\,\mathrm{V}$ represents the input signal. The remaining voltages are kept constant with $V_{\mathrm{min}}(t) = -U$ and $V_{\mathrm{max}}(t) = U$, where $U = 2\,\mathrm{V}$. A perfect clipper, with a much higher resistance, would clip the input signal between $\pm(U + V_{\mathrm{th}})$, where $V_{\mathrm{th}}$ is the threshold voltage of the diode. In the present case, it holds approximately $V_{\mathrm{th}} = 0.9\,\mathrm{V}$ such that the signal is between $\pm 2.9\,\mathrm{V}$. However, we have chosen the resistance such that the output signal should stay below 4 V.

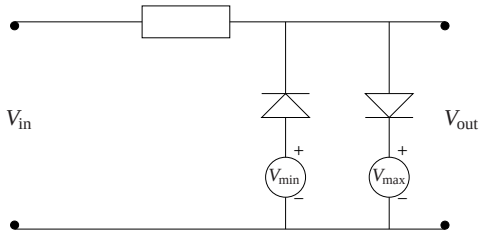


**Fig. 3** Clipper circuit with two *pn* diodes, one resistor and three voltages sources.

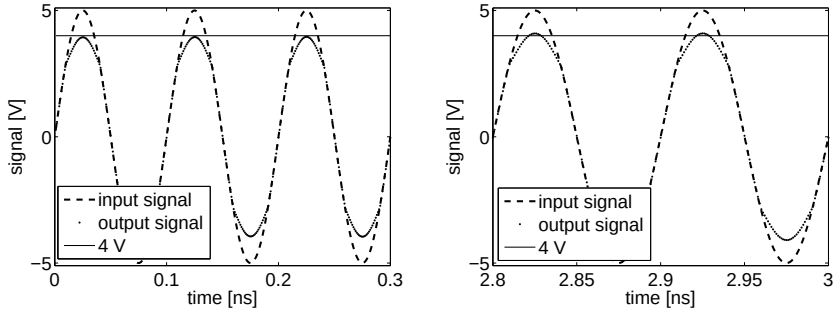


**Fig. 4** Input and output signal of the clipper during the first oscillations (left) and after 30 oscillations of the input signal (right).

In Figure 4 we depict the input and output signals of the circuit. We observe that during the first oscillations the maximal output signal is below 4 V, however, with a slight increase of the maximal value (left figure). The maximal output signal increases during the first oscillations from 3.93 V to 3.96 V. This increase becomes more significant for larger time (right figure). In fact, after 30 oscillations the maximal output signal is 4.09 V, which corresponds to an increase of about 5 %. A simulation of the same circuit with constant lattice heating keeps the maximum output signal almost constant below 4 V. This shows that the increasing maximal output voltage is caused by lattice heating, as the heated diode preserves less current leading to a larger resistance.

The circuit is constructed in such a way that, at the maximal input signal of 5 V, we have a voltage drop of about 1 V at the resistor, 2 V at the forward-biased diode and 2 V at the additional voltage source. In the branch containing the backward-biased diode, the voltage drop is 1 V at the resistor, 6 V at the diode, and $-2$ V at the additional voltage source. This behavior is illustrated in Figure 5. Thus, according to Figure 2 (right), we expect a stationary lattice temperature of about 360 K in the diodes. This is confirmed by the simulations presented in Figure 6 which shows the lattice temperature of one of the diodes in the circuit. We observe that the device heats up while being forward biased. As the backward bias period is to short to cool down the device, the lattice heating accumulates during the first oscillations up to about 360 K.

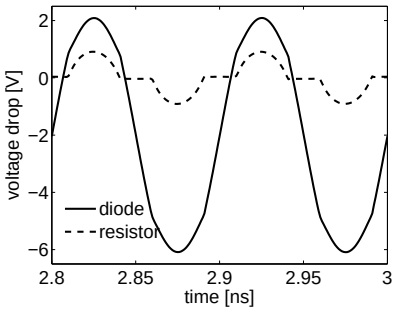


**Fig. 5** Voltage drop at the second diode and the resistor during the 29th and 30th oscillation.

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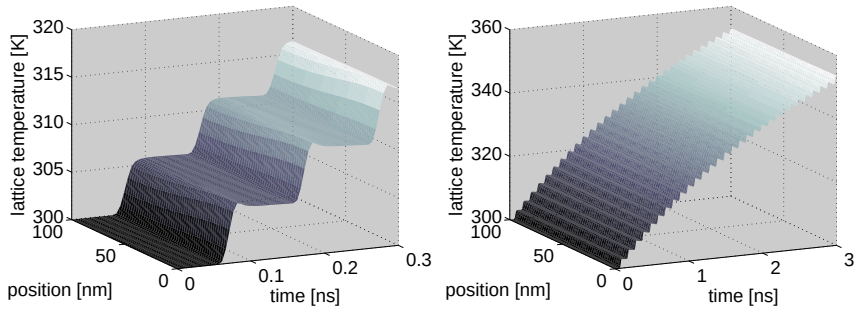


**Fig. 6** Distribution of the lattice temperature in one of the *pn* diodes within the first 3 (left) and within the first 30 (right) oscillations of $V_{\rm in}$.

## References


1. Adler, M.: Accurate calculations of the forward drop and power dissipation in thyristors. IEEE Trans. Electr. Dev., **25**, 16-22 (1978)
2. Albinus, G., Gajewski, H., Hünlich, R.: Thermodynamic design of energy models of semiconductor devices. Nonlinearity, **15**, 367-383 (2002)
3. Alì, G., Carini, M.: Energy-transport models for semiconductor devices and their coupling with electric networks. To appear in Proceedings of WSCP 2006 (2008)
4. Anile, A., Romano, V., Russo, G.: Extendend hydrodynamic model of carrier transport in semiconductors. SIAM J. Appl. Math., **61**, 74-101 (2000)
5. Bandelow, U., Gajewski, H., Hünlich, H.: Fabry-Perot lasers: thermodynamic-based modeling. In: J. Piprek (ed.), Optoelectronic Devices. Advanced Simulation and Analysis, pp. 63-85, Springer, Berlin (2005)
6. Bartel, A.: Partial Differential-Algebraic Models in Chip Design – Thermal and Semiconductor Problems. Ph.D. Thesis, Universität Karlsruhe, Germany (2003)
7. Ben Abdallah, N., Degond, P.: On a hierarchy of macroscopic models for semiconductors. J. Math. Phys., **37**, 3308-3333 (1996)
8. Brunk, M., Jüngel, A.: Numerical coupling of electric circuit equations and energy-transport models for semiconductors. SIAM J. Sci. Comput., **30**, 873-894 (2008)
9. Brunk, M., Jüngel, A.: Self-heating in a coupled thermo-electric circuit-device model. Preprint, Vienna University of Technology, Austria (2008)
10. Einwich, K., Schwarz, P., Trappe, P., Zojer, H.: Simulatorkopplung für den Entwurf komplexer Schaltkreise der Nachrichtentechnik. In: 7. ITG-Fachtagung “Mikroelektronik für die Informationstechnik”, Chemnitz, pp. 139-144 (1996)
11. Jüngel, A.: Transport Equations for Semiconductors. Springer, Berlin, to appear (2009)
12. Marini, L. D., Pietra, P.: New mixed finite element schemes for current continuity equations. COMPEL, **9**, 257-268 (1990)
13. Selberherr, S.: Analysis and Simulation of Semiconductor Devices. Springer, Berlin (1984)
14. Selva Soto, M., Tischendorf, C.: Numerical analysis of DAEs from coupled circuit and semiconductor simulation. Appl. Numer. Math., **53**, 471-488 (2005)
15. Tischendorf, C.: Topological index calculation of differential-algebraic equations in circuit simulation. Surv. Math. Industr., **8**, 187-199 (1999)
16. Tischendorf, C.: Coupled Systems of Differential Algebraic and Partial Differential Equations in Circuit and Device Simulations. Habilitation thesis, Humboldt-Universität zu Berlin, Germany (2003)
17. Wachutka, G.: Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling. IEEE Trans. Comp. Aided Design, **9**, 1141-1149 (1990)