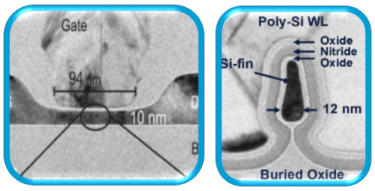

➢ Ultrathin Body and Multi-Gate Transistors for More Moore Electronics

The miniaturization of Field Effect Transistors (FET) for Logic and Memory applications highly depends on the effective control of short channel effects. To assess the scalability of specifc FET technologies, the concept of the *screening* or *natural length* λ in FET channels is commonly used. It is inspired from the Debye electrostatic screening length and is adapted to capture geometric and material features of the device studied in order to provide a metric for the gating efficiency of the channel. The intention is to derive the critical length along the charge transport direction required for the electronic bands of the semiconductor to react to the gate potential applied. The shorter λ is, the shorter the MOSFET channel length can be scaled without being critically affected by short channel effects.

A reduction of the MOSFET gate length below of ~ 30 nm requires an ultrathin thickness of the active semiconductor region and / or a multi-gate geometry embracing the active region. As seen in Fig 1. these transistor geometries deliver a reduced λ, the thinner the active region thickness t_{Si} is, the higher the dielectric constant is (use of high-k dielectrics) and finally the thinest the gate dielectric thickness t_{ox} is. Additionally, the higher degree of embracement of the gate electrode around the semiconductor region is given the smaller λ will be. Ideally, a nanowire or nanoslab geometry *completely surrounded* by a gate stack delivers the best scalability behavior of MOSFETs.

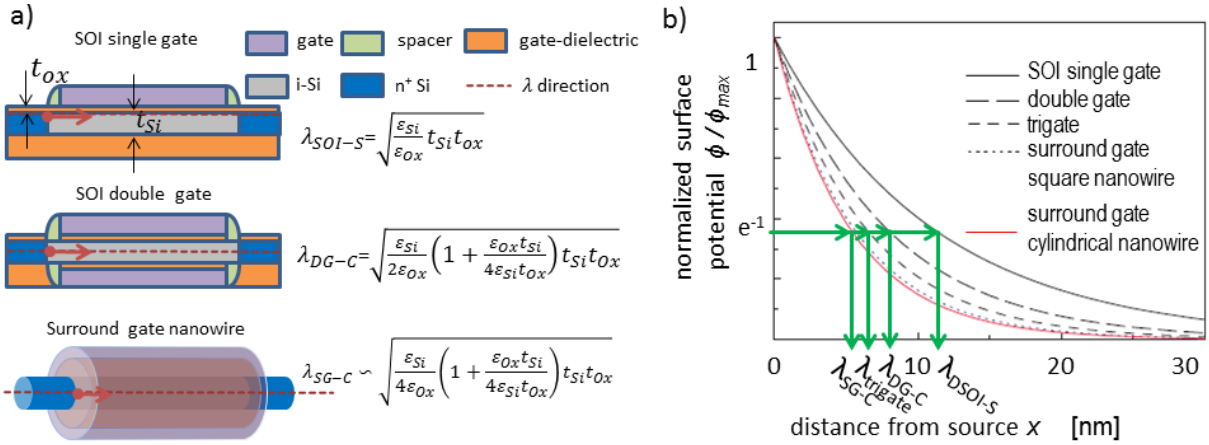

Figure 1. Potential $\phi(x)$ perturbation along the channel length for different FET geometries as described by the natural length λ. a) Natural length expressions for three different channel and gate geometries: Single gated SOI, double gated SOI and surround gated nanowire. The dashed line shows the direction where λ is calculated. b) Typical decay of potential over distance *x* from source along the channel length for different geometries in a). The screening length is the distance where the potential decays to the value of 1/e times of the initial value. Surround gate nanowire offers the lowest λ and best gate control over the channel, amongst all other implementations. From [1].

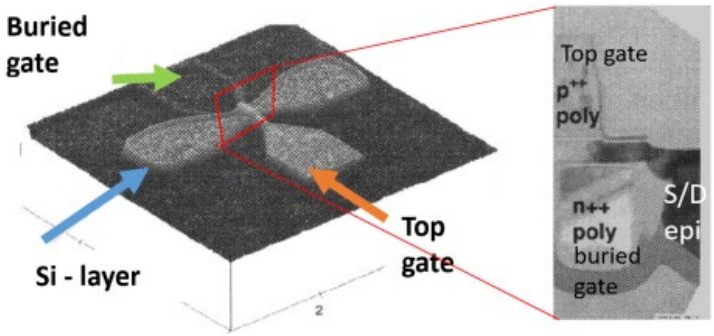

Fig. 2 More Moore nano-CMOS demonstrators. a) Recessed channel

The research experience of W. M. Weber started 2002 at the *Infineon Technologies AG – Corporate Research Labs* in Munich, Germany in the Nanodevices group of Dr. Lothar Risch with nanometer-scale **top-down** nanofabrication as well as semiconductor device technology of ultrathin-body silicon on insulator and multi-gate FETs. Thereto important contributions to build the **worldwide first bonded planar double gate transistor** [2] –Fig.2-,**fully depleted SOI FETs** (FDSOI) – Fig. 3a- [3] and **trigate-finFETs.** Moreover, the enhanced gate electrostatics enabled **trigate-finFET and nanowire FET flash memory cells with dual-bit operability** [4-5].

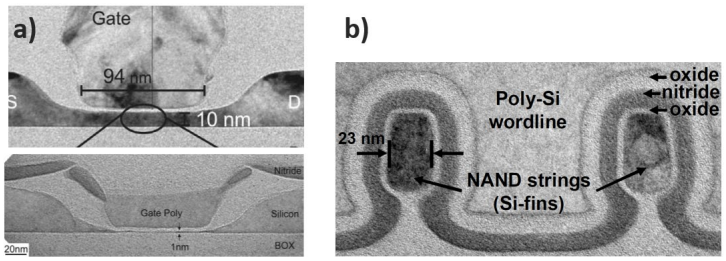

Fig. 3 More Moore nano-CMOS demonstrators. a) Recessed channel SOI MOSFET, b) Trigate fin-NAND flash memory cells IEDM 2006 .

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