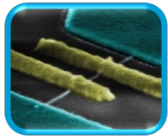


Research Achievements:



Reconfigurable Electronics

Emerging electronic systems in the field of data intensive applications such as *Edge Computing* and the *Internet of Things (IoT)* pose stringent demands in the computing power and energy efficiency of underlying integrated circuits. For these tasks the conventional CMOS scaling technology is reaching its outermost power consumption and performance limits and the *von Neumann Computing Architecture* is imposing a latency bottleneck in data transfer between memory and logic units. To leverage computational power beyond those limits the research field of *Reconfigurable Electronics* explores computational enhancement by extending the functionality of the basic switching units – the transistors – and thereby reinventing circuit topologies and memory-logic interaction.

The Reconfigurable Field Effect Transistor (RFET)

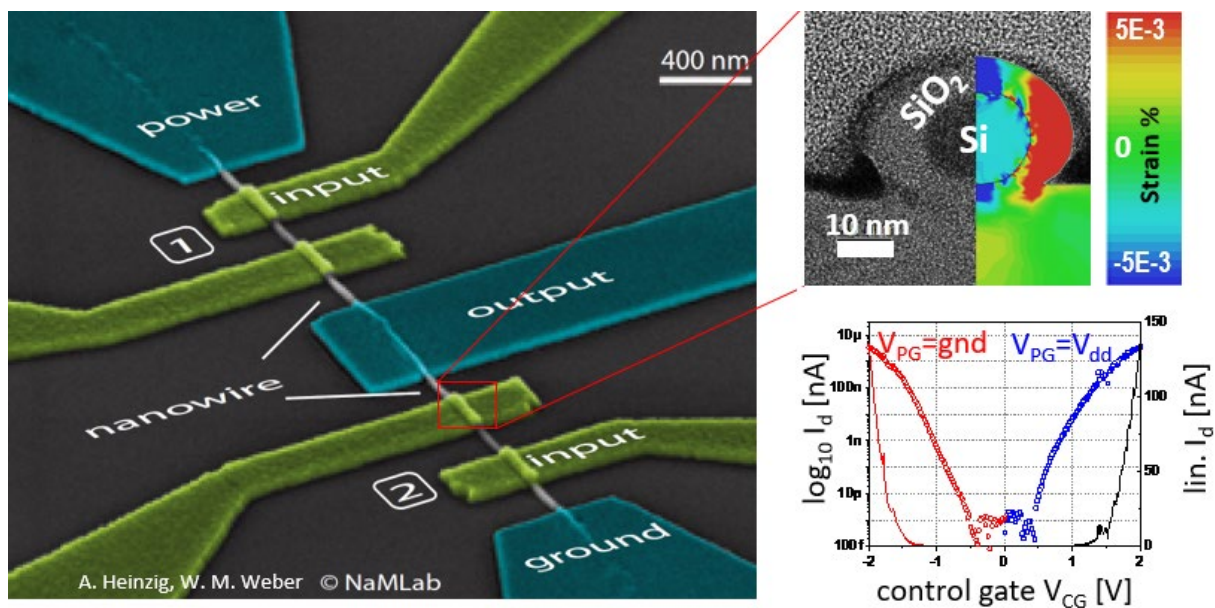


Figure 1. Reconfigurable silicon nanowire field effect transistor (RFET) implemented in a reconfigurable complementary inverter. RFETs reduce the complexity of n- and p-type FETs into a single and thus universal programmable transistor. Through strain engineering symmetric IV characteristics for n- and p-program can be achieved.

A promising *Reconfigurable Electronic* concept is the reconfigurable nanowire field effect transistor (RFET) – see Fig. 1– that provides unipolar n- or p-type electrical characteristics at runtime as programmed by an electric select signal. By exploiting reconfiguration at runtime, RFETs enable novel combinational and dynamic circuits that yield a higher number of functions with the same hardware complexity as conventional CMOS electronics. Importantly, RFETs do not require doping and can be entirely fabricated with materials and processes established in volume silicon and / or silicon-germanium CMOS production facilities.

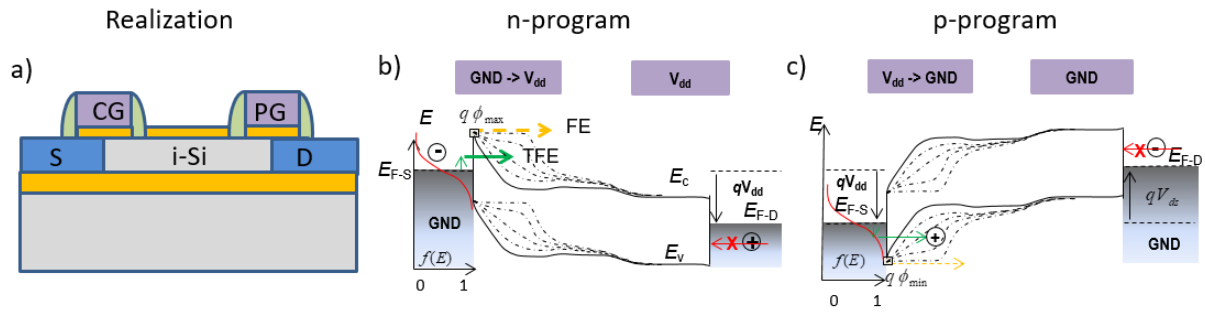


Figure 2. Operation principle of the RFET. a) physical structure with individually gated source (S) and drain (D) electrodes. Schematic band diagram of n- and p- program operation as adjusted by the potential of the program gate (PG) and control gate (CG) electrode.

RFETs were initially proposed and demonstrated by Walter Weber in 2006-2008 in the [Infineon Technologies AG Corporate Research](#) and later [Qimonda AG Material Research Laboratories](#) in Munich. Later Weber's group at [NaMLab gGmbH](#) in Dresden developed RFETs with strongly enhanced performance [[A. Heinzig et al. NanoLett 2012](#)] and was the first to demonstrate full circuit capability [[A. Heinzig et al. NanoLett 2013](#)] through its unique strain engineering approach to adjust the symmetry of the IV characteristics of n- and p-programmed FETs – Fig. 1-. Substantial performance enhancement and reduction in dynamic power consumption has been proposed through the use of germanium and silicon-germanium [[J. Trommer et. al. ACS Nano 2017](#)]. Latest developments have shown symmetric SOI based omega gate FETs [[M. Simon EDL 2020](#)] – Fig. 3- as well as first encouraging integration efforts in an industrial 22 nm FDSOI technology [[ESSDERC 2019](#)]. Recently, the demonstration of individually addressable non-volatile RFETs with multi-bit operability was undertaken with charge trapping gate stacks [[S.J. Park et. al. Adv. Elec. Mater. 2017](#)] and $\text{Hf}_x\text{Zr}_{1-x}\text{O}_2$ based ferroelectric gate stacks [[V. Sessi et al. Adv. Elec. Mater. 2020](#)].

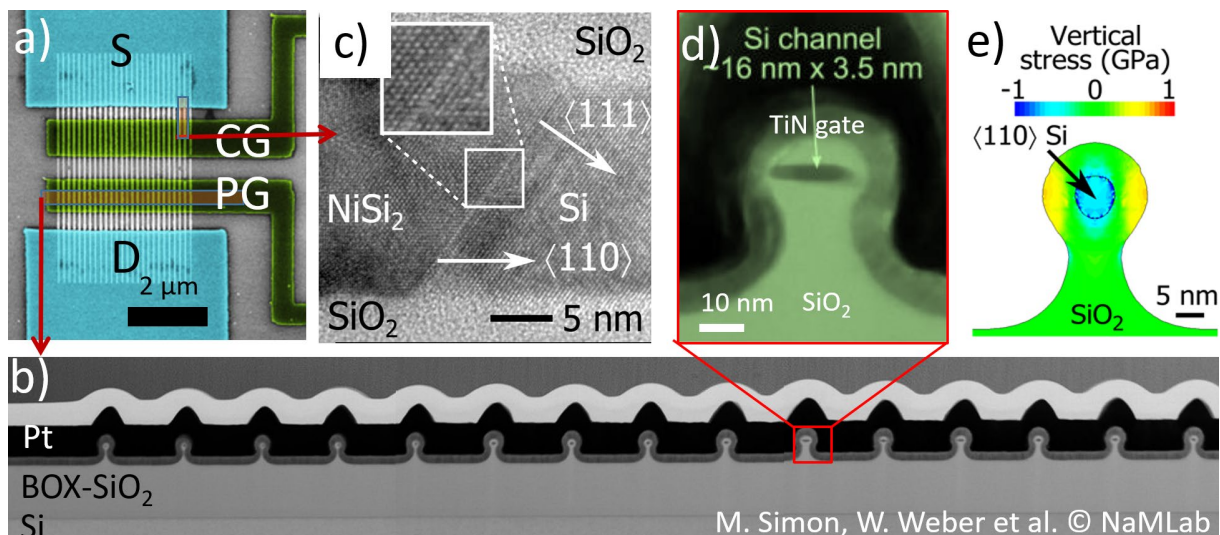


Figure 3. Top-down silicon on insulator (SOI) nanowire technology with omega shaped gate architecture. A recursive self-limited processing provides the controlled shrinkage of the Si nanowire / nanoslab core making diameters of thicknesses of ~ 3.5 nm accessible d) yielding excellent electrostatics and adjusts the required radial compressive stress e). a) Top view and

side cross-section b) and d). The NiSi₂ source channel Schottky junctions are flat and atomically abrupt enhancing the injection properties c).

At the circuit level the Weber Group at NaMLab showed reconfigurability of NAND / NOR / MIN circuit topologies [J. Trommer et al. EDL 2014] – Fig. 4 a-c- as well as XOR / XNOR runtime reconfigurability. [J. Trommer et al. DATE 2016] The RFET work was one of the key projects investigated within the German cluster of excellence [Center for Advancing Electronics Dresden](#) – cfaed-. There a complete and dedicated chain of models, logic circuit libraries, logic circuit synthesis for the automated design of deliberate combinatorial circuits was set up capable of even delivering the final technology layout for circuit fabrication (physical synthesis) –Fig. 4d- [S. Rai et al. DATE 2018]. With RFETs efficient multi-bit adders and arithmetic logic units (ALU) have been designed –Fig. 4e-.

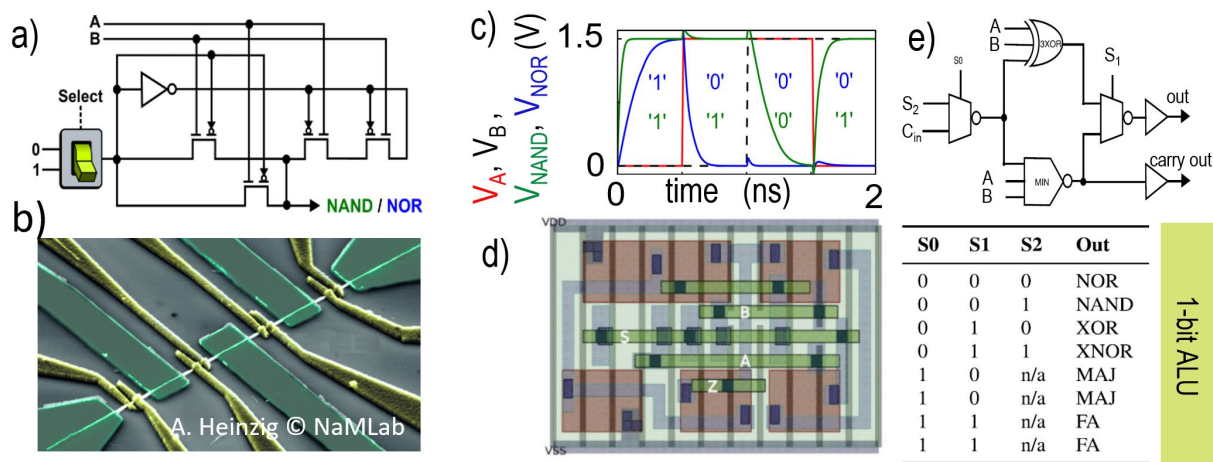


Figure 4. Reconfigurable circuits made of RFETs. Runtime reconfigurable NAND / NOR / MIN circuit: a) circuit, b) technical realization with a single nanowire, c) electrical performance showing equal delay for NAND and NOR functions, with respective layout in 22 nm FDSOI d). Single-bit arithmetic logic unit (ALU) built of RFETs incl. logic table e).

Read more on innovative nanometer scale silicon and germanium devices and RFETs in the following review articles:

[Silicon and Germanium Nanowire Electronics: Physics of Conventional and Unconventional Transistors](#)

W. M. Weber and T. Mikolajick

Reports on Progress in Physics (ROPP) **80**, 066502 (50pp) (2017)

DOI: 10.1088/1361-6633/aa56f0

[The RFET - a reconfigurable nanowire transistor and its application to novel electronic circuits and systems](#)

T. Mikolajick , A. Heinzig, J. Trommer, T. Baldauf and W. M. Weber

Semiconductor Science and Technology SST **32**, 043001 (17pp), (2017)

DOI: [10.1088/1361-6641/aa5581](https://doi.org/10.1088/1361-6641/aa5581)

[Reconfigurable Silicon Nanowire Devices and Circuits: Opportunities and Challenges](#)

[W. M. Weber](#)

Invited paper *IEEE Proc. Design, Automation and Test in Europe (DATE) 2014*

DOI: [10.7873/DATE.2014.249](https://doi.org/10.7873/DATE.2014.249)

[Reconfigurable nanowire electronics – A review](#)

[W. M. Weber](#), A. Heinzig, J. Trommer, D. Martin, M. Grube and T. Mikolajick

Invited paper *Solid State Electronics* **102**, pp. 12-24 (2014)