A Fully Integrated SPAD-Based CMOS Data-Receiver With a Sensitivity of −64 dBm at 20 Mb/s

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***Abstract*—A fully integrated 0.35-μm CMOS optical data receiver with a 50-μm diameter single-photon avalanche-diode and a cascoded gating circuit enabling a maximum excess bias voltage of 6.6 V (to obtain a high photon detection efficiency) is presented. To optimize the sensitivity in presence of dark counts and after-pulsing a decision threshold of 2–5 photon counts can be selected. For red light (635 nm) and nonreturn-to-zero modulation the sensitivity is −64 dBm for 20 Mb/s with 100 MHz clock frequency and −57 dBm for 50 Mb/s with 250 MHz.**

***Index Terms*—CMOS, optical data transmission, optical receivers, optoelectronic integrated circuit, single photon avalanche diode (SPAD).**

I. Introduction

Single photon avalanche diodes (SPADs) are avalanche photodiodes (APDs), which are capable of detecting single photons when operated beyond breakdown in Geiger mode. Important applications of SPADs are photon counters for quantum communication or highly sensitive image sensors. In [1], a 130-nm CMOS time-correlated photon counting 32 × 32 SPAD sensor for optical waveforms with XOR timing combiner and histogramming time-to-digital converter is reported with 16 GS/s throughput. In [2], a 64 × 64 pixel SPAD time-of-flight sensor in 150-nm CMOS for spacecraft navigation and landing is presented. SPADs, however, also are under investigation for the use in optical data receivers. In [3], a sensitivity of −31.7 dBm [bit error ratio (BER) = 10^{-9}] of a high dynamic-range receiver for 100-Mb/s nonreturn-to-zero (NRZ) and in [4] −55.7 dBm (BER = 2.10^{-3}) and −54 dBm (BER = 2.10^{-3}) for 50 Mb/s return-to-zero and NRZ, respectively, were achieved. With APDs in the linear mode a sensitivity (BER = 10^{-9}) of −38 dBm (λ = 860 nm) for 280 Mb/s [5] and a sensitivity (BER = 10^{-9}) of −34.6 dBm (λ = 675 nm) for 1 Gb/s [6] were reported.

This letter presents a compact, 0.35-μm CMOS optical data receiver, where only one SPAD instead of 1024 [3] and four SPADs [4] is implemented. The 50 μm diameter SPAD (breakdown voltage ∼30 V) has a similar structure as the APD presented in [6] and is controlled by a cascoded gating circuit. Because of a ∼12-μm low-doped *p*-epitaxial layer in this PIN-photodiode CMOS process, which works as a thick absorption zone, typically a higher quantum efficiency can be achieved compared to pure digital CMOS technologies with smaller structure sizes. The dark count rate (DCR) and the afterpulsing probability (APP) of the SPAD at excess bias V_{EX} = 4 V are 8000 s^{-1} and 2.5%, respectively. Beside a nonideal photon detection efficiency (PDE) and due to photon statistics, because of DCR and especially APP, detection of more than one photon is necessary for a logic one to achieve a low enough BER. Therefore, the pulse stream coming from the SPAD is fed from the comparator into a 5-tap shift register to evaluate five gating timeslots in a row per clock period. If at least 2, 3, 4, or 5 photon counts are detected (threshold) then a logical high is issued in this bit period. Possible applications are, e.g., indoor optical wireless communication or highly sensitive receivers for quantum cryptography.

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II. Circuit Description

In Fig. 1, the block diagram of the receiver is shown. The chip is supplied with V_{DD} = 3.5 V, V_{DDL} = 3.3 V, V_{SS} = −3.3 V, GND = 0 V, and V_{SUB} < −30 V. With V_{SPAD} and V_{SUB} the excess bias (V_{EX}) can be set up to 6.6 V, although the nominal supply voltage is 3.3 V in this 0.35-μm CMOS process. The excess bias is the voltage amount of the reverse voltage (V_{SPAD}–V_{SUB}), which exceeds the breakdown level. During reset (CLK = $\overline{\text{CLKD}}$ = 0 V), the cathode CAT is pulled down to V_{SS} by transistor N0 via cascode transistor N1 to set the SPAD voltage to a level below the breakdown voltage. Node PLS is switched to GND via N2. P1 (V_{casc}≈ − 1 V, adjustable) protects node PLS in that way that it cannot reach V_{SS} and to protect the transistors from large voltage differences. The transmission gate N4, P4 is turned off during reset of the SPAD (PLS connected to GND = 0 V, CAT ≈ V_{SS}).

For photon detection (CLK = 3.3 V, $\overline{\text{CLKD}}$ = −3.3 V) N0 and N2 are off, P0 charges nodes PLS and CAT to the potential V_{SPAD} and the reverse voltage of the SPAD (≈V_{SPAD}–V_{SUB}) is above breakdown (Geiger mode). P0 is turned off by the SPAD control when PLS is near V_{SPAD}. When a photon is detected, the SPAD pulls down node PLS to ≈0 V (limited by P1) and CAT to a voltage level at breakdown, which quenches the SPAD. Typically, such a voltage drop is in the order of the excess bias voltage (some volts) and fast (subns). Avalanches caused by dark counts and afterpulses (no photon detection) have the same behavior. N4 and P4 are on, so that during subsequent reset of the SPAD the state of PLS is stored dynamically at PLSSH and the photon is detected by the comparator. The first latch in the comparator (see Fig. 4) is in reset (metastable state of the first latch before decision) while the SPAD is active and transmission gate N4/P4 is on.

During reset of the first latch, the clocked inverters are switched off, and meanwhile, the previous decision of the comparator is held in the second latch. After an inverter buffer, the pulse sequence is applied to the 5-tab shift register (see Fig. 2). Every clock period a new pulse is fed into the shift register and the oldest one is discarded. Only if the number of counts out of five taps is greater or equal to a threshold, a logic high is issued per clock period by the decision blocks. For output $\overline{\text{DOUT}}$, the threshold 2, 3, 4 out of 5 counts can be chosen with the digital inputs DIG1 and DIG2. DOUT2 delivers a logical high only if 5 counts out of 5 are detected.

The control block for the SPAD is shown in Fig. 3. During reset of the SPAD (CLK = 0 V = $\overline{\text{CLKD}}$), $\overline{\text{LAT}}$ = CH = V_{DD}, LAT = 0 V, and PLS ≈ 0 V are present. Hence transmission gate P3/N3 is on,

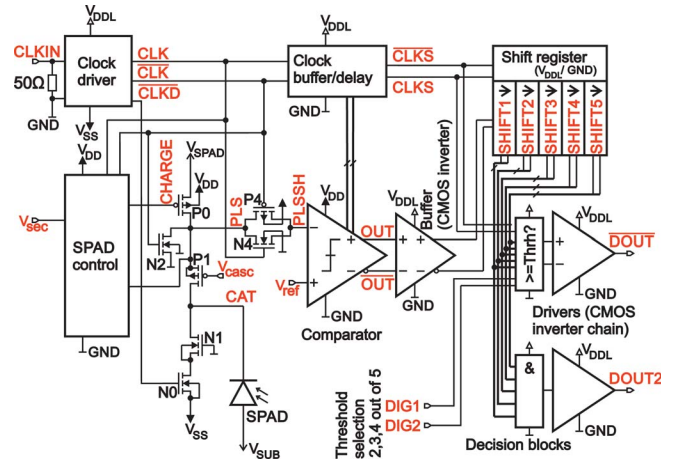

Fig. 1. Block diagram of the SPAD data receiver. N1 and P1 are cascode transistors to apply up to 6.6 V excess bias to the SPAD in this 3.3 V/0.35-μm CMOS technology.

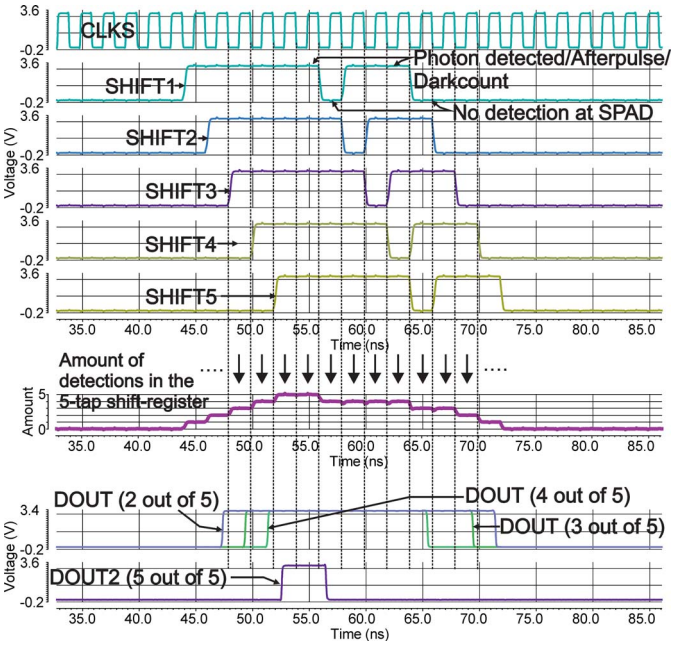

Fig. 2. Principle of operation of evaluating the pulse sequence from the SPAD to get DOUT and DOUT2. For a better understanding, DOUT instead of the inverted output $\overline{\text{DOUT}}$ is shown.

P2 is off, CHARGE = $\overline{\text{CLK}}$ = V_{DDL} = 3.3 V thus P0 is off. Transistors N0 and N2 are on. To set the SPAD for photon detection (CLK = 3.3 V, $\overline{\text{CLK}}$ = 0 V, $\overline{\text{CLKD}}$ = V_{SS} = −3.3 V), at the beginning $\overline{\text{LAT}}$ = CH = V_{DD} and LAT = 0 V, P3 and N3 are on, P2 is off and CHARGE = $\overline{\text{CLK}}$ = 0 V thus P0 is charging CAT and PLS until PLS reaches V_{SPAD}. The capacitance of the SPAD including surrounding parasitics is low enough, so that there is enough time for CAT and PLS to reach V_{SPAD} in the time between detection by N6 and turning off P0. Transistors N0 and N2 are turned off. Reaching V_{SPAD} turns on transistors N6, and hence, CH is discharged due to conducting N5. CH changes to 0 V, the latch switches to LAT = V_{DD} and $\overline{\text{LAT}}$ = 0 V, P3 and N3 are off, P2 is on and as a consequence CHARGE = V_{SPAD} thus turning off P0. The SPAD is ready for photon detection. If a photon hits the SPAD during charging node PLS by turned on P0, transistor N7 discharges CH to 0 V after a distinct time (adjusted with Vsec) to automatically turn off P0.

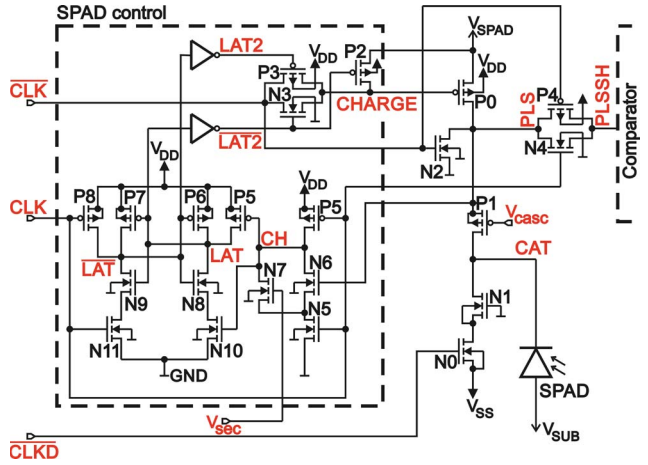

Fig. 3. SPAD control unit. The CMOS design avoids static power consumption (leakage currents neglected).

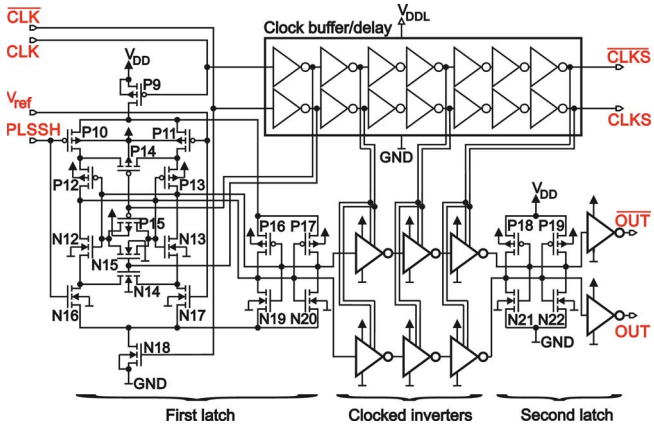

Fig. 4. Schematic of the clocked comparator with a second latch to store the decision during reset (SPAD quenched).

Fig. 4 shows the schematic of the comparator, which is capable of operating rail-to-rail at the input. During reset (CLK = 0 V), the first latch (cross coupled inverters N12–P12, N13–P13 with N19–P16, and N20–P17) is forced into a metastable state by reset transistors N14, N15, P14, and P15, while the supply rails are disconnected by N18 and P9. The clocked inverters between the first and second latch are off and the previous decision is stored in the second latch (cross-coupled inverters N21–P18 and N22–P19). When CLK changes to V_{DDL}, the reset transistors are turned off, transistors P9 and N18 connect the first latch to the supply rails and node PLSSH is compared with V_{ref}. In the case of a photon detection, the potential at PLSSH is lower than V_{ref}, the first latch switches accordingly and due to the turned on clocked inverters, OUT is pulled to V_{DD} by the second latch. In case of no photon detection OUT is set to 0 V.

PDE, dark counts, and afterpulsing are the main properties, which determine the sensitivity of the receiver. Once an avalanche is triggered, the voltage drop at the SPAD's cathode is in the order of the excess bias (some volts), and hence, a plenty of voltage difference is available (determined by V_{ref}) at the input of the comparator to have no serious influence of circuit noise. V_{ref} is adjustable to compensate for the offset of the comparator. All other parts of the circuit deal with digital CMOS voltage levels. Therefore, process variations are expected not to have an impact on the receiver's performance.

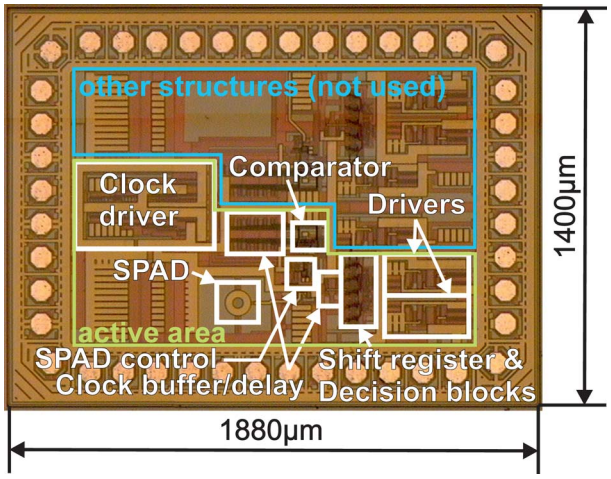

Fig. 5. Microphotograph of the fully integrated SPAD data receiver test chip. The active area of the receiver is 0.66 mm^2.

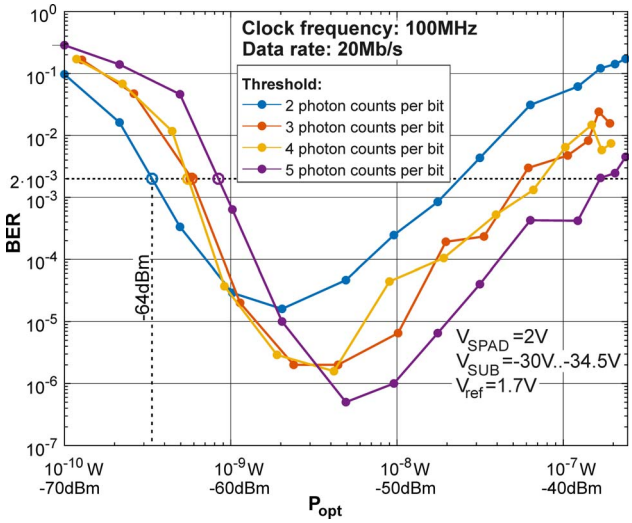

Fig. 6. BER measurements with an NRZ pseudo-random binary sequence (PRBS7) versus the mean optical power applied to the SPAD for different thresholds at 20 Mb/s.

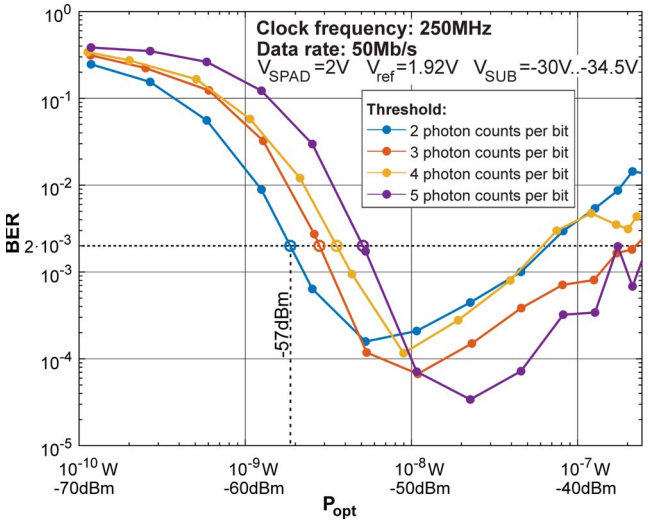

Fig. 7. BER measurements with an NRZ PRBS7 versus the mean optical power P_{opt} applied to the SPAD for different thresholds at 50 Mb/s.

III. Measurement Results

The optical receiver chip was fabricated in a 0.35-μm CMOS technology. A microphotograph is shown in Fig. 5. For measurements the receiver chip was bonded to a PCB, which was placed into a dark box on a peltier element to regulate the temperature to 25 °C. Around room temperature, the DCR varies approximately by a factor of 2 per 10 °C and becomes larger when the temperature is increased. The APP strongly depends on the excess bias as well as on the time duration, in which the SPAD is quenched below breakdown. If the reverse voltage is held constant, the temperature shift of the breakdown voltage, which rises by approximately 2 V per 10 °C, influences the PDE and the APP due to a change of the excess bias voltage. In the literature, there exists an on-chip circuit solution to hold the excess bias constant [8]. The SPAD was illuminated by a single-mode fiber with an NRZ pseudo-random-bit-sequence with length of 2^7-1 (PRBS7) externally modulated laser light [$\lambda = 635$ nm, extinction ratio (ER) > 100], where the data rate was one fifth of the clock frequency of the gating circuit in the receiver chip. V_{SUB} and V_{ref} were adjusted to minimize the BER. Here, the sensitivity is defined as the mean optical power (P_{opt}) being necessary on the SPAD to reach a BER of 2×10^{-3}. This value is sufficient to use a concatenated Reed-Solomon code super-FEC scheme to get a BER better than 10^{-9} with 6.69% redundancy (ITU-T G.975.1) [9].

The power consumption of SPAD control and comparator amounts to 7.2 mW for a clock frequency of 100 MHz and 13 mW for 250 MHz. A driver for a 50 Ω load consumes 120 mW at 250 MHz (50 mW@100 MHz) according to measurement. According to a simulation at 250 MHz the power consumption of the clock delay blocks, shift registers, and decision blocks amounts to 28 mW (12 mW@100 MHz). It is difficult to state a power consumption for a final optical receiver, because one of two 50 Ω drivers (CMOS inverter chain) could be saved easily in a final design. It also should be mentioned that the 50 Ω outputs were necessary for the bit-error characterization, but will not be needed for many applications.

Figs. 6 and 7 show measurement results of the BER versus the mean optical power (P_{opt}), which illuminated the SPAD, for 20 and 50 Mb/s. For 20 Mb/s, the best sensitivity was achieved with -64 dBm for a threshold of two photon counts per data bit. If the threshold is increased the sensitivity reduces to around -60 dBm, but better BERs of below 10^{-5} could be measured when increasing P_{opt}. A similar behavior was observed for 50 Mb/s, where the best sensitivity of -57 dBm was achieved for a threshold of two counts per bit. When increasing the threshold to five counts per bit the sensitivity reduces to -53 dBm, but a best BER of 3.2×10^{-5} at $P_{\text{opt}} \approx -47$ dBm is achieved. For higher optical power the influence of a limited ER can be observed resulting in a rising BER. Diffusion of electrons photo-generated in the substrate also may lead to a rising BER for increasing optical power.

IV. Discussion

Fig. 8 shows an illustration of the gap to the quantum limit of reported state-of-the-art results of APD and SPAD receivers and Table I provides a comparison. Here, the quantum limit is the mean optical power in dBm, which is needed by an ideal optical receiver to achieve a distinct BER due to the Poisson statistics of photons. It depends on the wavelength of the laser (λ) and data rate. For a BER of better than 2×10^{-3} at least seven photons have to be sent in average for a logical high [4].

The single-photon counting integrated receiver in [3] consists of a hierarchical 32 × 32 SPAD array. This array, where each SPAD had a diameter of 8 μm enables a large dynamic range of 79.1 dB

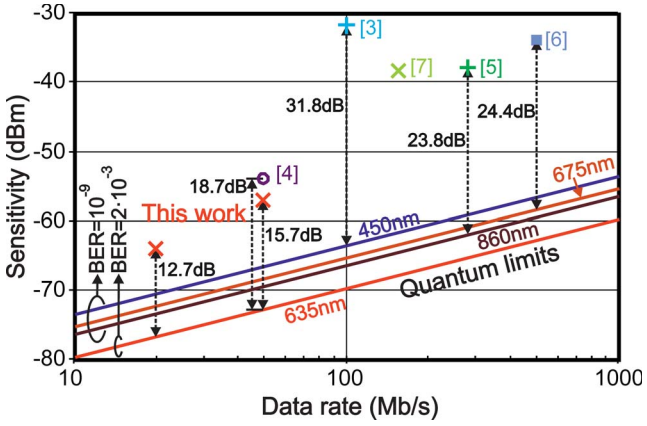

Fig. 8. Distance to the quantum limit of state-of-the-art results.

TABLE I
COMPARISON WITH REPORTED STATE-OF-THE-ART RESULTS

Ref	Technology Chip area	Data Rate	Sensitivity (BER) λ of laser	Photo-detector	Power Consumption
[3]	130nm CMOS 2.4×2.1 mm² [c]	100Mb/s	-33.6dBm [a] (10^{-6}) -31.7dBm [a] (10^{-9}) 450nm	32×32 SPAD array (each Ø 8µm)	max. 190mW
[4]	0.35µm CMOS 0.101mm² [e] 0.95 mm² [c]	50Mb/s	-54dBm [a] (2×20^{-3}) 635nm	4 SPADs (each 4174µm²)	min. 19.1mW [b]
[5]	discrete	280Mb/s	-38dBm (10^{-9}) 860nm	APD (Ø 1.95mm)	-
[6]	0.35µm CMOS 960×1540 µm² [c]	500Mb/s	-33.9dBm [a] (10^{-9}) 675nm	APD (Ø 0.4mm)	244mW
[7]	- -	155Mb/s	-38.5dBm (10^{-9}) -	APD (Ø 5mm)	-
This work	0.35µm CMOS 0.66mm² [d]	20Mb/s	-54dBm [a] (2×20^{-3}) 635nm	SPAD (Ø 50µm)	19.2mW [f] 119.2mW [g]
		50Mb/s	-54dBm [a] (2×20^{-3}) 635nm		41mW [f] 281mW [g]

[a] NRZ modulation of the laser
[b] Simulation result without considering SPAD events, four buffers (50Ω drivers) and external SPAD-pulse processing with MATLAB
[c] Whole die size including pads
[d] Active area
[e] Active area without four buffer for driving 50Ω
[f] Receiver without two 50Ω driver and clock driver
[g] Receiver including two 50Ω drivers

due to digital implementation consisting of counters and adders. The data rate of 100 Mb/s and a sensitivity of −31.7 dBm correspond to a gap to the quantum limit of 31.8 dB for BER = 10^{-9} and $\lambda = 450$ nm. An integrated optical receiver consisting of a 4-SPAD array is presented in [4]. After data analysis in MATLAB a gap of 18.7 dB for NRZ data was achieved. In [5], the discrete receiver used for optical wireless communication implemented an APD with 1.95 mm diameter. At a data rate of 280 Mb/s a sensitivity of −38 dBm (8B10B line coding) was reported, which results to a gap of 23.8 dB. The receiver chip of [6] in a 0.35-μm BiCMOS technology used an integrated 400-μm APD and achieved for 500 Mb/s a gap of 24.4 dB to the quantum limit. In [7], a large area Si-APD was used but no wavelength was stated. So no gap to the quantum limit could be calculated. With a 5 mm diameter Si APD, a receiver sensitivity of −38.5 dBm for a data rate of 155 Mb/s was measured [7]. Our presented optical receiver reduces the gap to the quantum limit to a value of 12.7 dB at 20 Mb/s and to 15.7 dB at 50 Mb/s.

V. CONCLUSION

The presented optical receiver comes closest to the quantum limit. For 20 Mb/s, the gap amounts to 12.7 dB being 6 dB better than in the state of the art. At 50 Mb/s, the sensitivity of −57 dBm is 3 dB better than the result for NRZ in [4], although only one SPAD instead of four SPADs is used. From the remaining gap to the quantum limit, we can derive a PDE of our SPAD of 21.5% (for two photons threshold and a 50% duty ratio of the gater).

REFERENCES

[1] N. A. W. Dutton *et al.*, "11.5 A time-correlated single-photon-counting sensor with 14GS/s histogramming time-to-digital converter," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, 2015, pp. 204–205.
[2] M. Perenzoni, D. Perenzoni, and D. Stoppa, "6.5 A 64×64-pixel digital silicon photomultiplier direct ToF sensor with 100MPhotons/s/pixel background rejection and imaging/altimeter mode with 0.14% precision up to 6km for spacecraft navigation and landing," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, 2016, pp. 118–119.
[3] E. Fisher, I. Underwood, and R. Henderson, "A reconfigurable single-photon-counting integrating receiver for optical communications," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1638–1650, Jul. 2013.
[4] H. Zimmermann, B. Steindl, M. Hofbauer, and R. Enne, "Integrated fiber optical receiver reducing the gap to the quantum limit," *Sci. Rep.*, vol. 7, Jun. 2017, Art. no. 2652.
[5] D. O'Brien *et al.*, "High-speed optical wireless demonstrators: Conclusions and future directions," *J. Lightw. Technol.*, vol. 30, no. 13, pp. 2181–2187, Jul. 1, 2012.
[6] T. Jukić, B. Steindl, and H. Zimmermann, "400 μm diameter APD OEIC in 0.35 μm BiCMOS," *IEEE Photon. Technol. Lett.*, vol. 28, no. 18, pp. 2004–2007, Sep. 15, 2016.
[7] M. J. McCullagh and D. R. Wisely, "155 Mbit/s optical wireless link using a bootstrapped silicon APD receiver," *IET Electron. Lett.*, vol. 30, no. 5, pp. 430–432, Mar. 1994.
[8] P.-H. Chang, C.-M. Tsai, J.-Y. Wu, S.-D. Lin, and M.-C. Kuo, "Constant excess bias control for single-photon avalanche diode using real-time breakdown monitoring," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 859–861, Aug. 2015.
[9] "Forward error correction for high bit rate DWDM submarine systems," Int. Telecommun. Union, Geneva, Switzerland, ITU-Recommendation G. 975.1, Feb. 2004.