IEEE Sensors Conf. 2020, pp. 1-4; doi: 10.1109/SENSORS47125.2020.9278771.

# Comprehensive Modeling of Photon Detection Probability in CMOS-based SPADs

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***Abstract*—Due to high sensitivity and CMOS compatibility, the single-photon avalanche diode (SPAD) is a promising optical detector in many applications. The sensitivity of a SPAD described by photon detection probability is a key parameter to be investigated. This paper presents a comprehensive model to characterize the photon detection probability of CMOS-implemented SPADs in technologies where an anti-reflection coating layer is not available. The model can accurately capture optical, photon absorption, and avalanche triggering effects. The obtained simulation results show a good agreement to our experimental evaluations and, therefore, the model can be reliably used to characterize the detection efficiency of CMOS SPADs for accurate device simulation and optimization.**

***Index Terms*—Single-photon avalanche diode (SPAD), Photon detection probability (PDP), Anti-reflection coating (ARC)**

## I. Introduction

DETECTING low-light signals down to single photon level and the integration into CMOS technology have made the single-photon avalanche diode (SPAD) the choice of photon detector in different applications [1]–[5]. A CMOS integrated SPAD structure uses an $\mathrm{n}^{+}$/p-well junction, where the depletion region extends down to the substrate layer to achieve a better performance [6]–[8]. An impinging photon absorbed in the depletion region generates an electron-hole pair and the electron can reach the multiplication region, where a strong electric field accelerates carriers to gain enough energy and create a self-sustaining avalanche. Such an avalanche process happens when the SPAD is reverse-biased above the breakdown voltage in the Geiger-Mode (GM).

Two key factors that characterize the performance of a SPAD are its intrinsic parasitics [9], [10] and the photon detection probability (PDP) [11]–[14]. In [9], we presented a statistical approach to characterize the SPAD parasitics including dark counts and after-pulsing. To characterize the PDP, a comprehensive model taking optical and electrical effects into account is needed as is explained later. This enables precise device simulation and provides insight into geometrical, wavelength and voltage bias dependencies of PDP as a key design parameter to achieve further improvements, for example, by engineering the electric field in the multiplication region [15]–[17].

Recently, a physics-motivated modeling and simulation approach has been presented to characterize the PDP based on the parameterization of the avalanche triggering probability (ATP) throughout the silicon [12]–[14]. As the ATP strongly depends on the depth in silicon (i. e. where an electron-hole pair is generated), an accurate absorption probability is necessary to characterize the PDP. This is especially important, when an anti-reflection coating (ARC) layer is not available as it is the case with many CMOS processes. In fact, as it is shown in this paper, the optical properties of SPAD structures without ARC are a complex function of wavelength and needs to be appropriately taken into account. Therefore, in this paper, we extend this approach to obtain a comprehensive PDP model which carefully combines optical and electrical simulations and captures the complex PDP wavelength dependencies.

To verify our model, the PDP spectrum of a SPAD with $\mathrm{n}^{+}$/deep-p-well (DPW) structure (Fig. 1) is calculated and compared with measured results. The reminder of the paper is organized as follows. Sec. II describes our SPAD and the proposed PDP model. It is explained how the absorption and avalanche triggering probabilities are obtained to calculate the PDP. Then, the simulated and measured results are presented and compared in Sec. III and finally, the paper is concluded in Sec. IV.

## II. Device and Model Description

### A. Device Structure

Fig. 1 shows the cross section of a SPAD fabricated with a $0.35\ \mu m$ standard high-voltage CMOS process. The photons coming from the top reach the silicon surface after passing through an isolation and passivation stack. When the device is biased beyond the breakdown voltage ($\mathrm{V}_{ex} = 6.6\mathrm{V}$), a strong electric field is formed in a thin zone at the interface of $\mathrm{n}^{+}$/deep-p-well defined as avalanche multiplication zone (shown in Fig. 2). To avoid edge breakdown, the $\mathrm{n}^{+}$ region is covered by a deep n-well and also the diameter of the deep p-well is formed to be smaller than that of the $\mathrm{n}^{+}$ region. The deep n-well is used to lessen the effective p doping of the deep p-well and p- epi layer which results in broadening

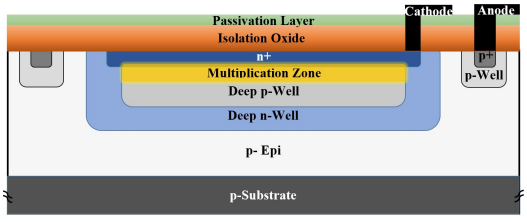


Fig. 1. Cross section of the $\mathrm{n}^{+}$/DPW SPAD (not to scale).

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the depletion region toward the p-substrate (Fig. 2). This remarkably widens the drift region where photons should be absorbed [6].

### *B. Photon Detection Probability Modeling*

PDP is experimentally obtained as the ratio of the detected photons to the total number of impinging photons measured using a (calibrated) reference detector. It is clear that a portion of the photons is reflected before reaching the silicon and only a part of the transmitted photons is absorbed and generates electron-hole pairs in an area which can result in an avalanche event. The optical transmission and the absorption profile depend on the wavelength ($\lambda$) as is shown in Fig. 3(a) and Fig. 3(b); the content of these figures is explained below. In a technology without ARC, the dependency of the optical transmission on $\lambda$ becomes a complex (fluctuating) function as is shown in Fig. 3(a). When a photon is absorbed inside the silicon, a self-sustaining avalanche event is not necessarily triggered. In fact, the avalanche triggering probability ($P_{\rm av}(x)$) defined as the probability that a photo-generated electron-hole pair initiates an avalanche event, is a function of the absorption depth ($x$) (i. e. the electric field) and the diffusion length of carriers ($L_{\rm e}, L_{\rm h}$) as they may recombine before reaching the drift and multiplication region.

Accordingly, the PDP is a function of both photon absorption probability ($P_{\rm ab}(\lambda, x)$) and avalanche triggering probability ($P_{\rm av}(x)$) and can be calculated as [11]

$$\mathrm{PDP}(\lambda) = \int_0^{\infty} \mathrm{P_{ab}}(\lambda, x) \times \mathrm{P_{av}}(x) dx. \tag{1}$$

In the following, it is explained how these probabilities are obtained to calculate the PDP.

*1) Photon Absorption Probability:* Conventionally $P_{\rm ab}$ is obtained as a function of wavelength ($\lambda$) and the penetration depth ($x$) using the following equation [12]–[14].

$$P_{\rm ab}(\lambda, x) = \alpha(\lambda) e^{-\alpha(\lambda) x}, \tag{2}$$

where, $\alpha(\lambda)$ is the photon absorption coefficient depending on $\lambda$. In order to model the PDP, however, this definition is not accurate enough to explain its complex wavelengths dependency (Fig. 3) in a CMOS SPAD without ARC. This is due to the formation of two standing waves in the isolation (oxide) and the passivation layers.

Fig. 3(a) shows the PDP and the optical transmission as a function of $\lambda$ obtained by measurement and using numerical solution of Maxwell equations with MATLAB, respectively.

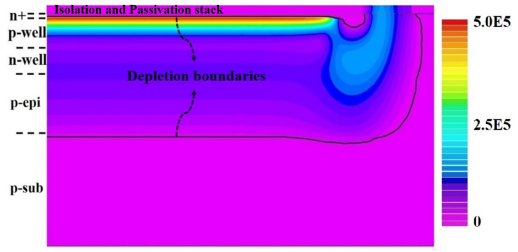


Fig. 2. Simulated 2D electric field profile and the depletion region boundaries in the $\mathrm{n^+}$/DPW SPAD at $\mathrm{V}_{ex} = 6.6$ V.

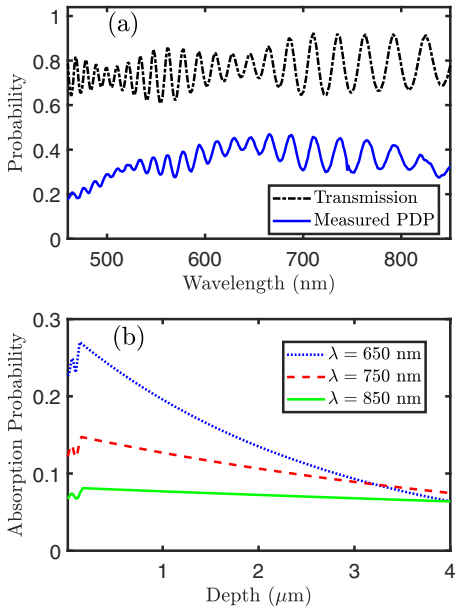


Fig. 3. (a) Obtained PDP and optical transmission using experimental and simulated results, respectively. (b) Photon absorption probability as a function of depth $x$ for different $\lambda$.

Fig. 3(b) shows the absorption profile inside the silicon as a function of depth for different wavelengths obtained numerically. Here, it can be seen that the photon absorption probability is not exactly exponential. In fact, due to the penetration of the standing wave from the isolation layer into the silicon, the exponential decay is shifted away from the silicon surface ($x = 0$) by ~200nm. In order to calculate the PDP accurately, it is important to take this effect into account. Especially in CMOS SPADs the multiplication zone is shallow and close to the surface (Fig. 2). Additionally, at short wavelengths a significant portion of arriving photons is absorbed close to the surface inside the silicon. For instance, at $\lambda$ from ~400nm to 500nm around half of the transmitted photons are absorbed within the depth range $x$ =0 to 200nm.

*2) Avalanche Triggering Probability:* According to Fig. 3(b), a photon can be absorbed either in the depletion layer (Fig. 2) or in the quasi-neutral regions above and below the depletion layer. In the case that a photon is absorbed in the depletion region, the generated electron and hole are promptly separated and accelerated in opposite directions. Thus, both electron and hole may initiate avalanche events, but due to the random nature of the impact ionization process, there is no guarantee that a self-sustaining avalanche will be established. The probability that an electron ($P_{\rm e}(x)$) or a hole ($P_{\rm h}(x)$) generated at the depth $x$ (within the depletion region) triggers a self-sustaining avalanche can be obtained by solving the following coupled equations [18].

$$\begin{aligned} \frac{\partial P_{\rm e}}{\partial x} &= (1 - P_{\rm e}) \gamma_{\rm e} (P_{\rm e} + P_{\rm h} - P_{\rm e} P_{\rm h}), \\ \frac{\partial P_{\rm h}}{\partial x} &= (1 - P_{\rm h}) \gamma_{\rm e} (P_{\rm e} + P_{\rm h} - P_{\rm e} P_{\rm h}). \end{aligned} \tag{3}$$

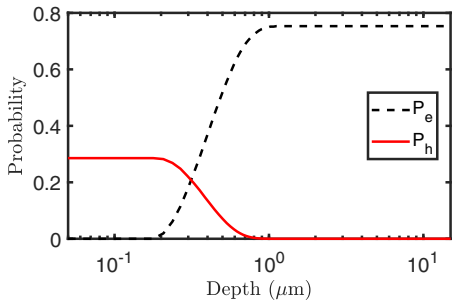


Fig. 4. Electron and hole avalanche triggering probabilities.

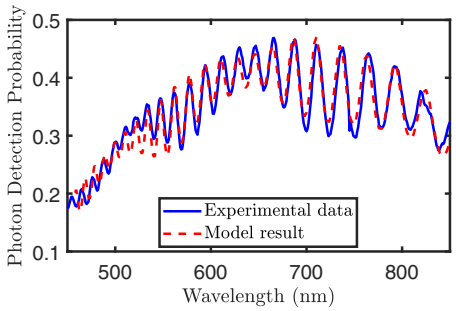


Fig. 5. Measured and simulated PDP as a function of $\lambda$.

Here, $\gamma_{\rm e}$ and $\gamma_{\rm h}$ are the electron and hole impact ionization coefficients, respectively. The electron and hole avalanche triggering probability distributions are shown in Fig. 4. Here, it can be seen that inside the depletion region and below the multiplication zone ($x$ from $\sim$0.8$\mu$m to 10$\mu$m) $P_{\rm e}(x)$ has a constant value. This is due to the fact that an electron generated at any $x$ in this region, will pass across the whole multiplication region to reach the cathode through $\rm n^+$. On the other hand, when the electron is generated above the multiplication region, it is transferred towards the cathode without flowing through the multiplication region and, thus, $P_{\rm e}$ is equal to zero close to the silicon surface. It is clear that for electrons generated inside the multiplication region ($x$ from $\sim$0.2$\mu$m to 0.8$\mu$m), $P_{\rm e}$ increases with $x$ from zero to a maximum value. A similar argument applies to the holes but in a reverse manner with $x$ as the holes are transferred towards the anode. Due to a smaller impact ionization coefficient associated with the holes compared to that of the electrons, the maximum value of $P_{\rm h}$ is smaller than the maximum $P_{\rm e}$. In the case a photon is absorbed outside the depletion region (i. e. the neutral region below or above the depletion region), the generated carriers may result in an avalanche if they diffuse into the depletion region. For the neutral region below (above) the depletion region, a diffusing electron (hole) only can result in an avalanche if it passes through the multiplication region. For such electron (hole) that diffused into the depletion region, the avalanche triggering probability is equal to the maximum $P_{\rm e}$ ($P_{\rm h}$) value. However, not every carrier would diffuse into the depletion zone from the neutral regions. Therefore, we need to take the recombination probability into account to obtain the total avalanche triggering probability.

Up to now, we have considered the avalanche triggering probability corresponding to electrons ($P_{\rm e}$) and holes ($P_{\rm h}$) as a function of $x$ in the different regions. Accordingly, the total avalanche probability when a photon is absorbed at $x$ ($P_{\rm av}(x)$), is obtained in accordance with the probability that either an electron or a hole triggers an avalanche (as two independent events) and is given by

$$P_{\rm av}(x) = [P_{\rm e}(x) + P_{\rm h}(x) - P_{\rm e}(x)P_{\rm h}(x)] \times P_{\rm diff}(x). \quad (4)$$

This can be used to calculate the PDP based on Eq. 1. One should note that $P_{\rm diff}(x)$ depends on the diffusion length in the neutral regions and is equal to 1 in the depletion region.

## III. Model and Experimental Comparison

We have measured the PDP of a SPAD with $\rm n^+$/deep-p-well structure (Fig. 1) for different wavelengths at an excess bias voltage of 6.6V and room temperature. To count the detection events, a NI-PXI system coupled with LabView was used. Photons of flux $5 \times 10^6$(photons/s) are incident on the 85$\mu$m diameter SPAD through a 62.5$\mu$m multimode fiber coupled with a monochromator which swept the wavelength from 450nm to 850nm by steps of 1nm. The PDP is calculated based on the model explained above. This model accurately captures all optical transmission, photon absorption, and avalanche triggering effects. The electron and hole avalanche triggering probabilities as well as the depletion region boundaries are precisely simulated using the Geiger-mode device simulation feature of SILVACO Atlas [19]. To extract the photon transmission and absorption profile inside the structure, Maxwell equations are solved numerically.

The measured and simulated results (at $\rm V_{ex} = 6.6$ V) are compared in Fig. 5. The $\lambda$-dependent fluctuations in the PDP as a result of the formation of two standing waves in the isolation and passivation stack is captured in our numerical simulation. In general, a good consistency between experimental and simulated results is obtained and we believe that this model can be reliably used to characterize and optimize the PDP of CMOS SPADs based on accurate device modeling and simulation. Furthermore, this model can be used for more accurate modeling and optimization of optical devices where SPADs are used as photon detectors [20].

## IV. Conclusion

A comprehensive model is presented to characterize the PDP performance of CMOS SPADs. It is shown that due to a complex dependency of PDP on wavelength, an accurate optical characterization of the device structure is necessary. This is more critical when an anti-reflection coating is not available in the CMOS technology. A good agreement between our experimental and simulated results is demonstrated. The presented model can be used for accurate PDP characterization and proves useful to considerably reduce the time and cost required for experimental-based characterization and optimization in different CMOS SPAD applications.

## Acknowledgment

The authors acknowledge financial support from the Austrian Science Fund (FWF, grant no. P28335-N30).

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