Single-Photon Avalanche Photodiode Based Fiber Optic Receiver for Up to 200 Mb/s

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(Invited Paper)

***Abstract*—The first fully integrated receiver based on single-photon avalanche diodes (SPADs) for data rates of up to 200 Mb/s is reported. An array of four SPADs in combination with quenching circuits and a short dead time of 3.5 ns is fabricated in a 0.35 μm CMOS process. The responses of the SPADs are combined using an integrated digital latch-type processing circuit to create a single output data stream. In addition, the output of each quenching circuit is recorded and the bit error rates are extracted by post-processing in MATLAB. Using a 635-nm single-mode laser source, the bit error rate at different optical power is measured at 50, 100, 150, and 200 Mb/s. The integrated digital circuit achieved the best sensitivity at –46.3 dBm (BER = $2{\cdot}10^{-3}$) for 100 Mb/s. Using the MATLAB postprocessing, a sensitivity of –43.8 dBm at 200 Mb/s (BER = $6.5{\cdot}10^{-3}$) is reached.**

***Index Terms*—Optical receivers, optoelectronic integrated circuit, optical data transmission, single-photon avalanche diode.**

I. Introduction

USING avalanche photodiodes (APDs) in the linear mode instead of standard PIN photodiodes is a common practice to improve the sensitivity of optical receivers [1]. Two wire-bonded APD receivers for visible light communication are reported in [2]. The fast receiver achieved a sensitivity of −34 dBm at 1.25 Gbit/s (850 nm). The second receiver for room scale coverage achieved a sensitivity of −38 dBm at 280 Mbit/s (850 nm).

In order to reduce the influence of parasitic components and because of low cost production aspects, it is important to integrate the APD and the circuits on a single chip (optoelectronic integrated circuit, OEIC).

A monolithically integrated analog high sensitivity receiver using a 200 μm diameter avalanche photodiodes with a transimpedance amplifier is reported in [3]. It shows a fully integrated receiver fabricated in 0.35 μm CMOS for optical wireless communication with a sensitivity of −31.8 dBm at 1 Gbit/s, measured with a 670 nm laser source. An integrated receiver with a 400 μm APD with a sensitivity of −34.6 dBm at 1 Gbit/s (675 nm) is reported in [4].

The major limiting parameters of these receivers regarding sensitivity are the excess noise of the APD in the linear mode (amplification noise) and the electronic noise of the circuits. Operating the APD in the Geiger mode leads to a much higher gain than in the linear mode and therefore eliminates excess noise of the APD and electronic noise. The utmost theoretical limit of the sensitivity of an SPAD-based optical receiver is the quantum limit, set by the Poisson statistics of the incoming photons [5]. For proper comparison of the reported results in [2]–[4], the quantum limit at a bit error rate (BER) of 10^{-9} for 1.25 Gbit/s, 1 Gbit/s and 280 Mbit/s relates to −55.4 dBm (850 nm), −55.3 dBm (675 nm) and −61.9 dBm (850 nm), respectively. This clearly points out that there is still a rather wide gap towards the quantum limit.

Avalanche photodiodes operating in Geiger mode, i.e. above the breakdown voltage (V_{bd}), may help to build receivers with better sensitivity. These so-called single-photon avalanche diodes (SPADs) generate detectable output signals even by the absorption of single photons. A quenching circuit is needed for the SPAD to stop the self-sustaining avalanche to be sensitive for further incoming photons again. Passive or active quenching reduces the operating voltage below V_{db} for a certain time (dead time, t_d). After t_d the SPAD is set to the active state again by increasing the operating voltage to the initial value.

Parasitic effects of the SPAD, however, limit the sensitivity for such a receiver. Several effects like dark counts, afterpulsing and optical crosstalk lead to unwanted output pulses, which contribute to the BER [6].

SPADs have been used as detectors for quantum key distribution [7]. The first integrated SPAD-based optical receivers were published in [8] und [9]. In [8] a 32 × 32 SPAD array is used to achieve a sensitivity of −31.7 dBm at 100 Mbit/s and 450 nm wavelength where the quantum limit is at −63.6 dBm. The major goal of [8] was to achieve a large dynamic range. An array of 100 SPADs is used in [9] for 20 Mbit/s, unfortunately no sensitivity was reported.

In [10] a pulse amplitude modulation technique (4-PAM) is used to achieve a sensitivity of −64 dBm at 100 kbit/s with a 32 × 32 SPAD array fabricated in 0.13 μm CMOS where

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the quantum limit is at −95 dBm. In [11] a 1024 SPAD array with an orthogonal frequency multiplexing technique was used to achieve a sensitivity of −107 dBm at 1 kbit/s where the quantum limit is at −115 dBm.

In [12] and [13] completely different approaches to increase the sensitivity of optical receivers using superconducting nanowire detectors (SNSPD) are reported. Due to the high detection efficiency, large spectral range, low dark count rates and excellent timing performance those receivers were especially used for free-space optical communication for infrared wavelength. Data rates up to 781 Mbit/s are reported in [12] using NbN-nanowires at a temperature of 2 K. Since the uncoded BER saturates at 0.1, a rate-1/2 serially concatenated pulse-position modulation (SCPPM) forward error correction (FEC) code is used to achieve error-free communication for 8 and 20 photons per bit at 781 Mbit/s and 390 Mbit/s, respectively. This corresponds to sensitivities of −61 dBm and −60 dBm for a wavelength of 1550 nm. A mid-IR single-photon receiver for 100 Mbit/s free-space optical communication is presented in [13]. Unfortunately, no sensitivity is reported. However, due to high fabrication costs and cryostatic operating temperatures those receivers are not suitable for low-cost light communication systems and are therefore not considered in comparisons in the remaining text.

In [6] an array of only four SPADs with separate absorption and multiplication zone in combination with cascoded quenching circuits and a dead time of 9 ns was used to achieve sensitivities of −55.7 dBm at 50 Mbit/s and −51.6 dBm at 100 Mbit/s with 635 nm light. The quantum limit is at −72.8 dBm and −69.7 dBm, respectively, for a BER of 2×10^{-3} at 635 nm wavelength. Two different methods of data processing with MATLAB of the output signals of the four channels for the BER extraction were reported: a digital latch-type and an analog processing method.

Here, we report a speed improved SPAD receiver consisting of four SPADs combined with a cascoded quenching circuit having a total dead time of only 3.5 ns and an integrated digital latch-type processing output circuit.

The major goal was to design the first fully integrated SPAD based receiver for bit rates up to 200 Mbit/s. This paper reports the structure and the measurement results of the sensitivities at 50 Mbit/s, 100 Mbit/s, 150 Mbit/s and 200 Mbit/s. For proper comparison, the sensitivities are extracted with the integrated digital circuit and with MATLAB using a digital latch-type processing method.

II. Receiver Structure

In this section, we discuss the SPAD's structure and the performance of the SPAD array regarding dark count rate (DCR), afterpulsing probability (APP) and optical crosstalk probability (OCTP) as well as the structure of the complete receiver chip.

A. SPAD Array

The structure of the integrated SPAD described here was originally reported as linear-mode APD, fabricated in 0.35 μm CMOS with a maximal bandwidth of 1.15 GHz [14]. In [4] and [15] this general structure of APD is used in an optoelectronic integrated circuit (OEIC) for VLC systems. The APD consists of a separate thick p-epitaxial absorption zone and a multiplication zone at the interface of the n++ cathode and the p-well. The top view, the cross section and the distribution of the electric field is shown in Fig. 1(a).

An APD with the same layer structure is also used for the SPAD array in [6]. The photon detection probability PDP was 22.4% with a quenching voltage of 3.3 V and 36.7% at 6.6 V quenching voltage both for 635 nm light [6]. Since the doping regions used here are the same as in [6], the PDP of the SPADs in the receiver reported here should be equal. However, compared to [6] the total active area of the array is 2.8 times smaller with the aim of decreasing the DCR and the APP because of the expected increase of APP for the shorter dead time. To ensure that only the light sensitive parts of the SPAD are illuminated with the incoming light beam, a metal shield is introduced to cover the inactive regions.

The total area of the array is about 0.018 mm^2. The light spot diameter was adjusted to be slightly smaller than the diameter of the p-well to use the full photon sensitive area of approximately 0.0053 mm^2 as efficiently as possible. Considering the area of the light spot of about 0.011 mm^2 the fill factor of the presented structure results in 0.48, compared to 0.53 of the array reported in [6].

Fig. 1(b) and (c) show surface scans at two different heights of the single mode fiber tip (core diameter ~ 4 μm) above the chip surface scanning the SPAD array. Both figures are measured at the same excess bias voltage (V_{ex}) and at constant optical power of approximately 100 pW. For these measurements, the count rates of all four SPADs were recorded simultaneously while scanning the SPAD with the fiber in x/y directions.

The shape of the SPADs can be seen at the lower distance of approximately 100 μm (Fig. 1(b)). The count rate is normalized to the peak value of the channel with the highest count rate. As can be seen the count rate of all four SPADs are in the same range, indicating that the photon detection probability of the four SPADs are comparable.

Increasing the distance of the fiber to the surface, results in an increased diameter of the light spot, resulting in illumination of all 4 SPADs at the same time, if the spot is kept in the center of the array. Fig. 1(c) shows the sum of the count rate of all four SPADs at a fiber distance of 570 μm. The distance of the fiber was optimized, so that all 4 SPADs show almost the same count rate, and the sum of the count rate of the 4 SPADs becomes a maximum. In our setup, this optimum distance was 570 μm. The extracted effective fill factor results in 0.44.

The DCR, the APP and the OCTP for all four SPADs over the used V_{ex} range (range for the sensitivity extraction of the receiver) are shown in Fig. 2. The break down voltages of three SPADs is approximately 27.8 V. This Voltage is used to define the excess bias voltage for this SPAD array. SPAD3 shows a larger breakdown voltage of 28.2 V.

As expected, compared to the results in [6], all parasitic effects are increased, because of the strongly reduced dead time (3.5 ns) necessary to improve the maximum data rate of the quenching circuit.

This results in a reduced maximum excess bias voltage usable for the receiver. As can be seen in Fig. 2, the DCR as well as the

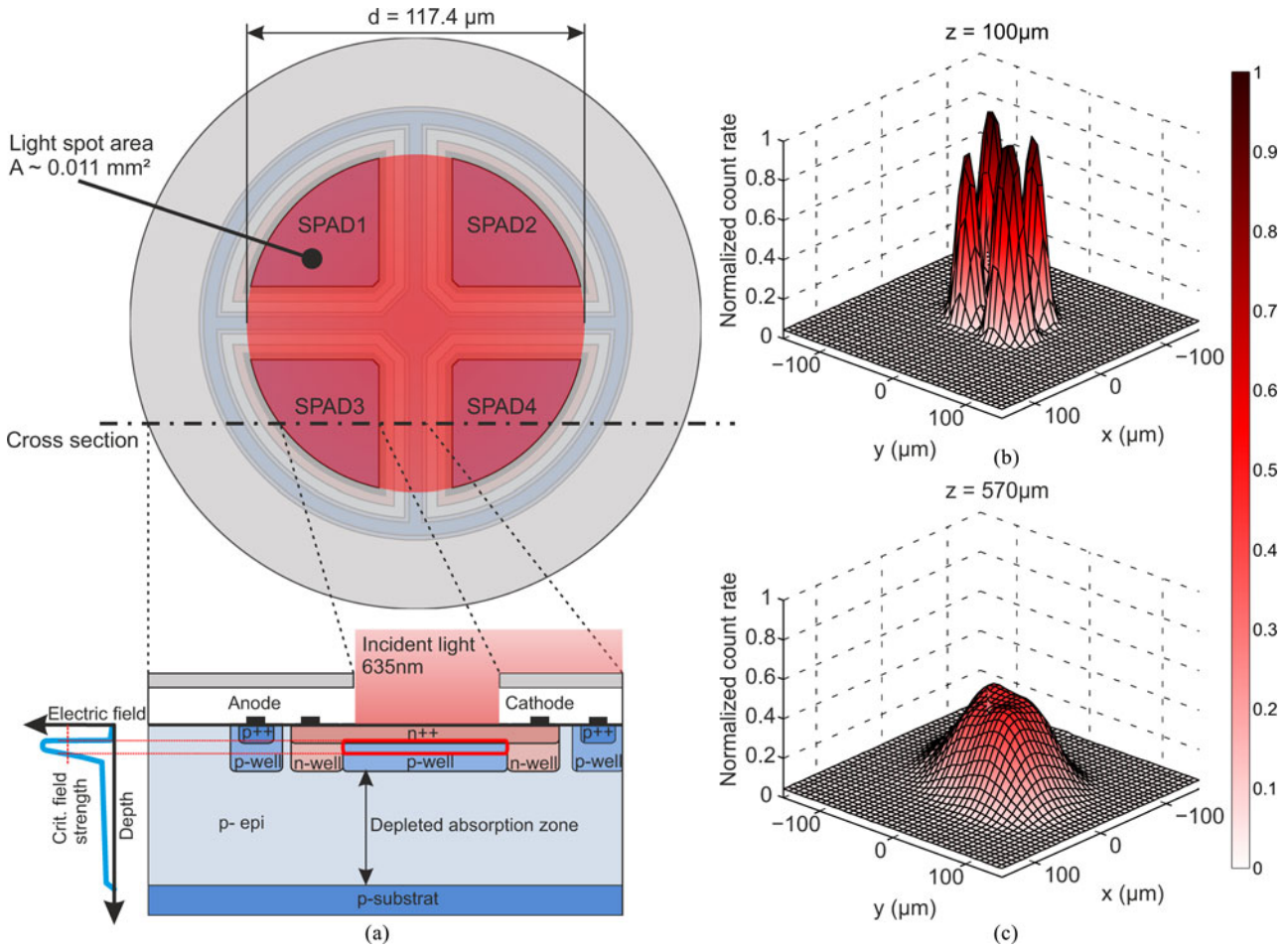

Fig. 1. Structure of the SPAD array. (a) Upper part: top view (not to scale), lower part: cross section and schematic electric field distribution (not to scale). (b) Surface scan with fiber tip ~120 μm above chip surface (c) Surface-scan with fiber tip ~1 mm above chip surface.

APP increase rapidly above 3 V excess bias voltage. Fig. 2 additionally shows that the DCR is different for different channels. Comparing all SPADs, SPAD3 has the largest DCR. It ranges from 6,600 s^{-1} at $V_{ex} = 1.5$ V up to 13,900 s^{-1} at $V_{ex} = 3.5$ V. SPAD4 shows the best DCR characteristics with 1,460 s^{-1} at $V_{ex} = 1.5$ V and 8,960 s^{-1} at $V_{ex} = 3.5$ V respectively.

As reported in [16] the APP strongly depends on the dead time. This can be explained by the lifetime of trapped carriers, which is in the same timescale as the dead time of the quenching circuit [16]. Even for higher excess bias voltages, after the

SPAD is set to the active state again, these "free" carriers can trigger an additional avalanche called afterpulse. The slope of the APP curves (Fig. 2) is almost uniform up to $V_{ex} = 2.5$ V (at $V_{ex} = 2.5$ V APP is 18%). At $V_{ex} = 1.5$ V the APP is approximately 12% for all SPADs. The APP for SPAD3 is shifted to the right because of the higher break down voltage. Therefore it shows the minimal APP of 28% at $V_{ex} = 3.5$ V. The maximal APP at $V_{ex} = 3.5$ V is 56% for SPAD1 and SPAD4.

The optical crosstalk probability between two SPADs is also shown in Fig. 2. An event is called optical crosstalk if two or more SPADs generate an output pulse at the same time (within 1 ns out of the "dark" measured data). As it can be seen, the four curves representing the crosstalk between direct neighbors (for instance SPAD1 and SPAD2) are very similar. The probability for a diagonal optical crosstalk (between SPAD1 and SPAD4 and between SPAD2 and SPAD3) is clearly reduced. The OCTP between three SPADs is less than 0.5% for the used excess bias voltages. For this range of operation, an optical crosstalk between all four SPADs at the same time is not recorded, even at a V_{ex} of 3.5 V.

B. Receiver

A representative block diagram of the complete receiver is shown in Fig. 3. As mentioned in the previous section the SPAD array consists of four individual SPADs. Every SPAD is connected to a cascoded quenching circuit (CQC) with a low detection threshold of 100 mV to reduce the total avalanche charge. Due to the implemented cascoded structure, the quenching voltage (equivalent to the maximal possible excess bias voltage) is doubled up from 3.3 V (regular supply voltage) to 6.6 V. The performance and the structure of the quenching circuit is discussed in [6].

The theory of operation for the quenching circuit used for this receiver is still the same and therefore not discussed in detail. The dead time of 9 ns used in [6], was insufficient for the aim of

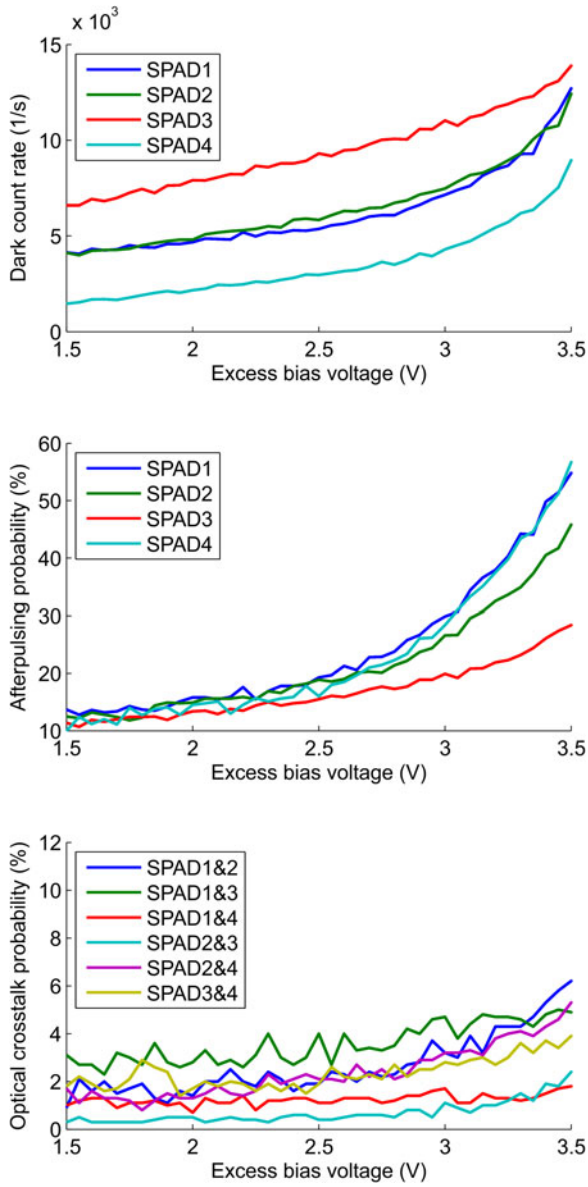

Fig. 2. DRC, AQC and OCTP (between 2 SPADs) at 25 °C.

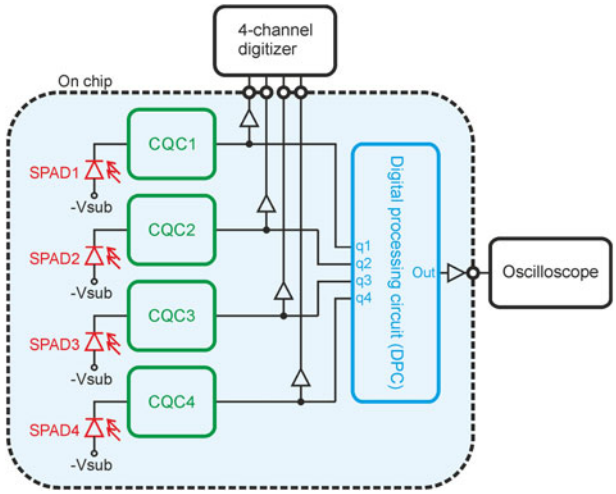

Fig. 3. Block diagram of the receiver chip and the connections of the outputs of the cascoded quenching circuits to the 4-channel digitizer and of the output of the digital processing circuit to the oscilloscope.

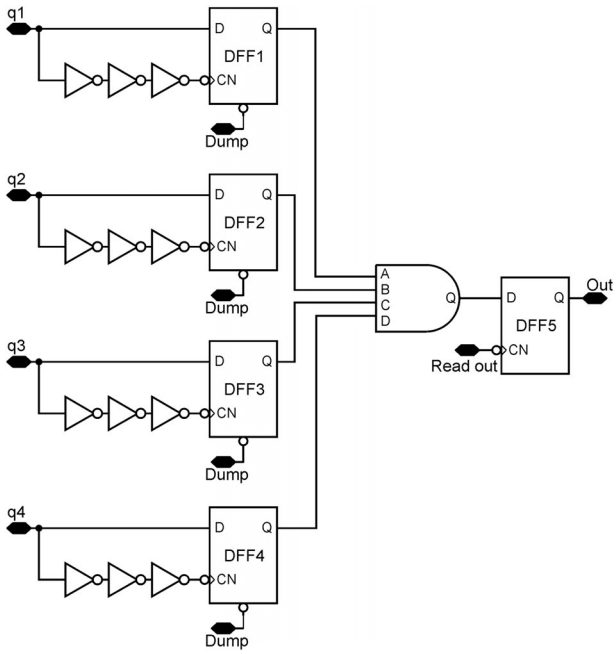

Fig. 4. Schematic diagram digital latch-type processing circuit.

receiving data signals up to 200 Mbit/s. Therefore, the total dead time of the optimized circuit was reduced to 3.5 ns by improving the sequencer and the logic elements in the CQCs. The time between detection of a photon and quenching completely is the same as in [6], i.e. 1.0 ns. To the authors best knowledge this is the shortest reported dead time of a quenching circuit so far.

As shown in Fig. 3 all of the CQCs are connected to a digital latch-type processing circuit (DPC). In Fig. 4 this digital circuit is shown in more detail. The outputs of the quenching circuits for each SPAD are connected to the inputs *q1* to *q4* of the DPC. These inputs are fed to the data inputs, as well as via three inverters to the clock inputs of the following D-Flip-Flops (DFF1 to DFF4, respectively) to generate a falling edge at the clock input in order to latch an incoming "1". DFF1 to DFF4 are enabled during the bit and are reset at the end of the bit using the *Dump* inputs. The output signals of the D-Flip-Flops are combined by a logical "AND" gate and fed to the single D-Flip-Flop (DFF5) for read-out. The read out is done shortly (1.5 ns) before the reset of the latches to optimize the sensitive time of the circuit. The output signal is connected to a 50 Ω buffer for driving the input of the oscilloscope. The output is a logical "1" only if all inputs of "AND" are "1" before the read out.

For characterisation of the data stream from each individual SPAD without the digital processing circuit, each CQC is also directly connected via a 50 Ω buffer to a 4-channel digitizer.

The microphotograph of the receiver chip is shown in Fig. 5. The total dimension is 1400 × 1040 μm^2. Each quenching circuit has a dimension of 130 × 130 μm^2 without blocking capacitors and without the output buffer. The total area of the digital block is 0.014 mm^2 also without buffer and blocking capacitors.

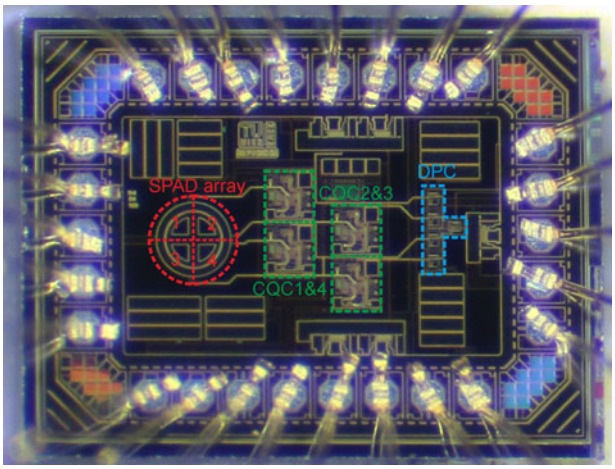

Fig. 5. Microphotograph of the receiver chip.

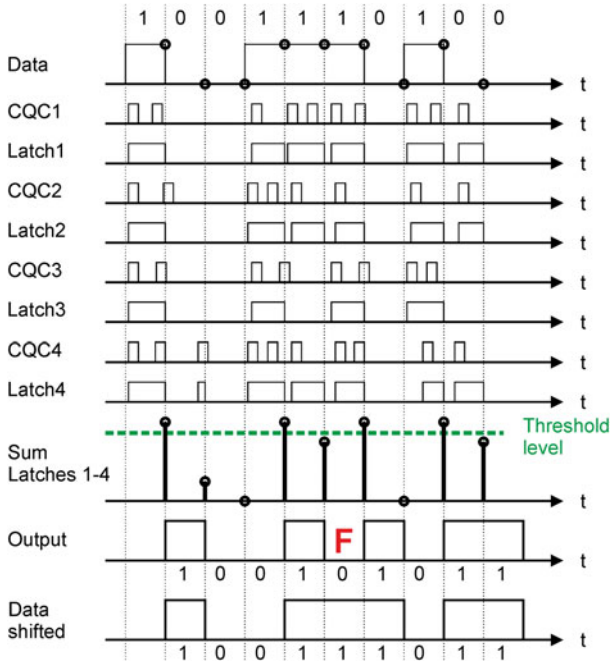

Fig. 6. Principle of digital latch-type processing of the 4 active quencher circuits (AQC) output data. The final output data are shifted by one bit period to the right compared to the input data.

The total area of the chip is mainly determined by the number of pads necessary for the two different output types and therefore increased compared to [6]. However, in principle the additional buffers and the pads for the direct output of the quenchers are not necessary for operation. Removing them, of course would save a considerable amount of chip area. The mean power consumption of a single CQC over the complete dead time (3.5 ns) after a SPAD event occurs is 12.3 mW. In idle state, it is approximately 6.2 mW. The DPC consumes a power of 0.6 mW during a logical "1" and 15.2 μW for a "0" at its output, equivalent to an average power of 0.31 mW per bit.

III. Experimental Results

This section shows the experimental results of bit error measurements. As explained above, the receiver offers two possibilities for the extraction of the data. In the experiments, the received bit streams were recorded before and after the integrated digital processing circuit. For all measurements shown in this section, the receiver chip was mounted in a dark box and set to a temperature of 25 °C.

As shown in Fig. 1 the light spot diameter of the used optical single-mode (SM) fiber was set to a slightly smaller diameter compared to the diameter of the active area using a motorized x/y/z-stage to have nearly the same amount of light density on each SPAD. The incoming light was generated by a 635 nm SM laser source. This light source includes an external modulator for supporting an extinction ratio larger than 100. An optical attenuator allowed sweeping the optical power, while an internal monitoring photodiode was used to monitor the optical output power. Before aligning the fiber tip above the SPAD array, the mean optical power was measured by an optical power meter (Thorlabs PM200). The laser was modulated by a return to zero (RZ) signal using a pseudo random bit sequence (PRPS 7). It is reported in [6] that a reduced duty ratio of the RZ results in a lower BER. This can be explained due to the fact that bit errors caused by the jitter of the SPAD can be strongly reduced if the period during a bit during which photons hit the SPAD is reduced. Especially at 200 Mbit/s where the bit duration is only 5 ns this jittered pulse might cause an error for a following logical "0". Therefore, a duty cycle of 20% was used for all measurements shown in this section. The excess bias voltage was optimized for every BER reported in this section. The BER is determined by post processing using MATLAB. The recorded output data stream is compared to the reference PRBS-7 input signal. Each bit is sampled in the center, as it is done in common bit pattern receivers. All errors are counted and the BER is derived by dividing the total number of errors by the total number of the received bits [6].

As shown in Fig. 3, a 4-channel digitizer (NI PXIe-5162) was used to measure the output data of the 4 CQCs. The extraction of the bit error rate from these four data streams was done by a digital latch-type processing method in MATLAB as described in detail in [6]. A LeCroy Waverunner 204Xi oscilloscope was connected to the output of the integrated DPC.

A. Digital Latch-Type Processing With MATLAB

For a combined output stream of the four quenching circuits, a latch-type processing method was emulated using MATLAB. This method was presented in [6]. For each channel, the received bit stream was stored in 2 blocks of 12.5 ms duration for the used data rates. This corresponds to 1.25 million bits for 50 Mbit/s und 5 million bits for 200 Mbit/s, respectively. The principle of this method is depicted in Fig. 6. Within a bit period, the latches of each channel are set by a positive edge of the input signal. The state of the latch is stored until the end of every bit. The output is set to high state if the number of latches supporting a logical "1" is higher than the threshold level. The resulting output stream is shifted by a bit period compared to the input stream. For an easier comparison, also a shifted version of the input stream is depicted in the bottom of Fig. 6. The bit error shown in Fig. 6 arises because in this example SPAD3 does not detect a photon within the bit duration due to the limited PDE, a too low optical input power or a too low excess bias voltage.

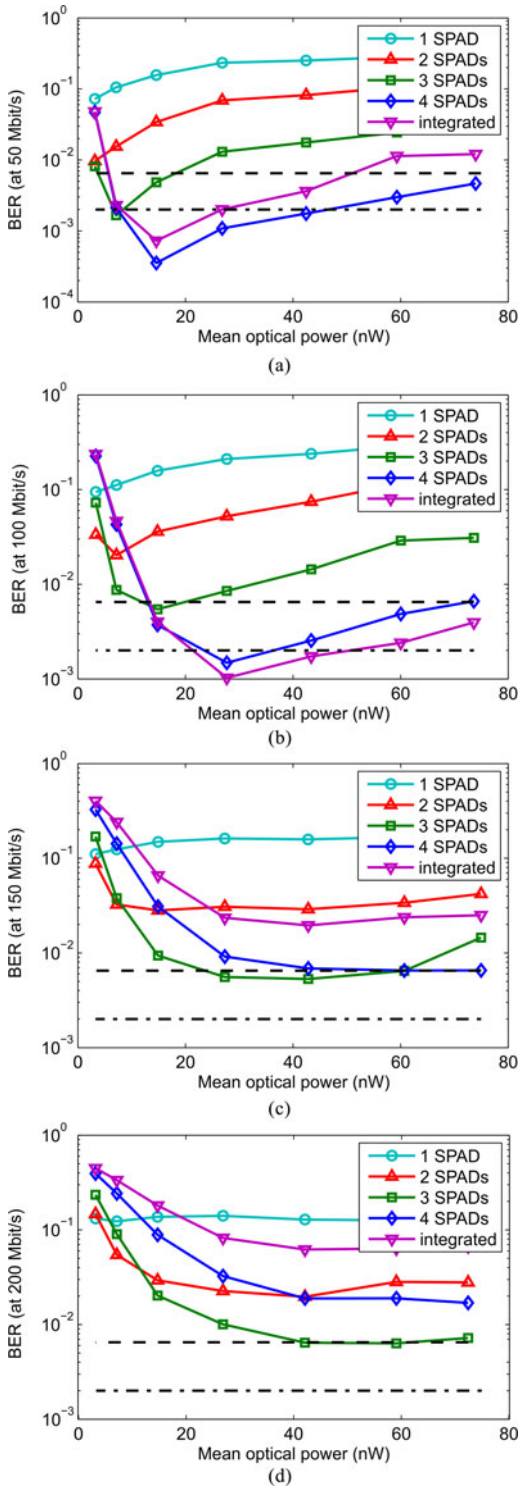

Fig. 7. BER at different optical power of the incident light; (a) 50 Mbit/s (b) 100 Mbit/s (c) 150 Mbit/s (d) 200 Mbit/s.

The resulting BER for 50 Mbit/s (a), 100 Mbit/s (b), 150 Mbit/s (c) and 200 Mbit/s (d) depending on the optical power of the incident light is shown in Fig. 7. Each graph shows four different curves for the digital processing, showing the different threshold levels. For example the top most curve "1 SPAD" shows the corresponding BER, if a logical "1" is achieved when one or more SPADs are triggering during a bit, while for curve "4 SPADs" all four SPADs need to trigger during one bit in order to get a logical "1" at the output.

As can be seen the best BER for 50 Mbit/s and 100 Mbit/s is achieved at a threshold level of 4 (pulses in all 4 SPADs are necessary during one bit to detect a logical "1").

The best BER at 50 Mbit/s is $3.5 \cdot 10^{-4}$ at an optical power of 14.5 nW (−48.4 dBm). A BER of $2 \cdot 10^{-3}$ is required for using forward error correction to achieve an output BER of 10^{-9} using concatenated Reed-Solomon (RS) and product code as reported in [17]. A BER of $2 \cdot 10^{-3}$ is indicated by the dashed line in the sub figures of Fig. 7. The sensitivity (at a BER of $2 \cdot 10^{-3}$) for 50 Mbit/s is at −51.2 dBm (7.6 nW). For 100 Mbit/s, the best BER of $1.5 \cdot 10^{-3}$ is at −45.6 dBm (27.7 nW) optical power. A BER of $2 \cdot 10^{-3}$ is reached at −46.1 dBm (24.7 nW).

At 150 Mbit/s, the best BER of $5.3 \cdot 10^{-3}$ is reached at −43.7 dBm (42.8 nW). For 200 Mbit/s, the best BER is $6.3 \cdot 10^{-3}$ at −42.3 dBm (59.0 nW) optical power. As can be seen the BER does not reach the $2 \cdot 10^{-3}$ level for these data rates. However, using a forward error correction code with higher error correction capability (e.g., RS(255,239)/CSOC (n0/k0 = 7/6, J = 8) super FEC code as shown [17]) a BER of $6.5 \cdot 10^{-3}$ is sufficient for an output BER of 10^{-9}, with the drawback of a 24.48% redundancy necessary for the iterative CSOC decoding. For 150 Mbit/s and 200 Mbit/s a BER of $6.5 \cdot 10^{-3}$ is achieved at −46.1 dBm (24.3 nW) and at −43.7dBm (42.8 nW), respectively.

B. Integrated Digital Processing Circuit

The BER for the integrated processing circuit is also included in Fig. 7. As described in the previous section the integrated digital processing circuit operates in general like the MATLAB processing method at a threshold level of 4 (neglecting the timing of the clock inputs). The characteristic for the BER at 50 Mbit/s and 100 Mbit/s for the integrated processing and the MATLAB processing (at a threshold of 4) are therefore in the same range. The sensitivity (at a BER of $2 \cdot 10^{-3}$) is at −51.4 dBm (7.2 nW) for 50 Mbit and at −46.3 dBm (23.5 nW) for 100 Mbit/s respectively.

For 150 Mbit/s and 200 Mbit/s the best BER of $1.9 \cdot 10^{-2}$ is achieved at −43.7dBm (42.8 nW) and $6.2 \cdot 10^{-2}$ at −43.8dBm (42.1 nW), respectively. The main reason for that is the "threshold level". As it can be seen in Fig. 7, the 3 out of 4 method achieves better results in MATLAB at higher data rates (150 Mbit/s, 200 Mbit/s). In the chip, however, a 3 out of 4 processing circuit is not implemented. It would of course be easy to include such an output in a future chip. Furthermore, the dead time during the read out of the integrated circuit consumes already a considerable amount of the bit time, resulting in a worse BER.

IV. Discussion

With respect to the extraction method (MATLAB or integrated) the best results of the BER for data rates from 50 Mbit/s up to 200 Mbit/s are summarised in Fig. 8.

As reported in the previous section the latch-type MATLAB method achieves the best BER characteristic at 50 Mbit/s, 150 Mbit/s and 200 Mbit/s. As can be seen for 100 Mbit/s the

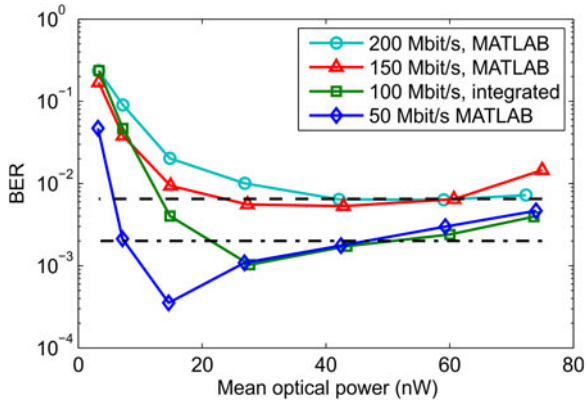

Fig. 8. Summary of the best BER results for 50 Mbit/s, 100 Mbit/s, 150 Mbit/s and 200 Mbit/s.

BER of the integrated circuit is slightly better than the characteristic of the MATLAB method. During the 1.5 ns necessary for the read out, the output of the integrated DPC is not sensitive for pulses generated by the quenching circuits. This can avoid errors caused by parasitic effects (for instance dark counts) during a logical "0". However, this effect should also be seen for 50 Mbit/s. As it can be seen in Fig. 7(a) this is not the case. However, the sensitivity of both methods is almost identical.

The error sources limiting the BER for high and low optical power are different. As can be seen in Figs. 7 and 8, the curves immediately start to decrease by increasing the optical power. If the optical power is too low, the number of photons during the "1" is too low to be correctly detected by the receiver. Main possibility to improve the BER in this range of optical power is to increase the PDP.

After passing a minimum, the BER starts to increase for increasing optical power. Responsible for this is that the probability for the correct detection of a logical "0" decreases. We think, main reasons for this is the finite extinction ratio of the light source and the avalanches triggered by "slow" carriers caused by diffusion generated in the substrate. Due to the finite extinction ratio of the source, the number of photons during the "0" increases for higher optical input power. The carriers diffusing from the substrate are mainly generated during the "1" by photons that are absorbed in the substrate.

From an error correction perspective the worst-case scenario is a burst of errors caused by a train of after pulses, crosstalk or a combination of both. However, the used concatenated FEC codes provide a high burst error correction capability [17].

A comparison of the linear interpolated sensitivities is shown in Table I. The best BERs for 150 Mbit/s and 200 Mbit/s are achieved at a threshold level of 3 SPADs per bit. A possible explanation for that might be that the dead time after a pulse generated by parasitic effects avoids the detection of an incoming logical "1". Therefore, the possibility that 4 SPADs can detect the incoming photons during shorter bit durations decreases (even for low duty cycles of the RZ-signal).

A comparison of the state of the art for high sensitivity receivers is shown in Fig. 9. The dashed line in this figure represents the resulting limit of the sensitivity for integrated (Bi)CMOS receivers using an APD in linear mode ([6], derived from the best sensitivity reported so far [4]). The quantum limit

TABLE I
COMPARISON OF THE SENSITIVITY

BER	processing Method	Data rate (Mbit/s)	Sensitivity (dBm)
$2\cdot10^{-3}$	MATLAB 4 SPADs	50	−51.2
$6.5\cdot10^{-3}$	MATLAB 4 SPADs	50	−51.7
$2\cdot10^{-3}$	Integrated 4 SPADs	50	−50.7
$6.5\cdot10^{-3}$	Integrated 4 SPADs	50	−51.7
$2\cdot10^{-3}$	MATLAB 4 SPADs	100	−46.1
$6.5\cdot10^{-3}$	MATLAB 4 SPADs	100	−48.5
$2\cdot10^{-3}$	Integrated 4 SPADs	100	−46.3
$6.5\cdot10^{-3}$	Integrated 4 SPADs	100	−48.4
$6.5\cdot10^{-3}$	MATLAB 3 SPADs	150	−46.2
$6.5\cdot10^{-3}$	MATLAB 3 SPADs	200	−43.8

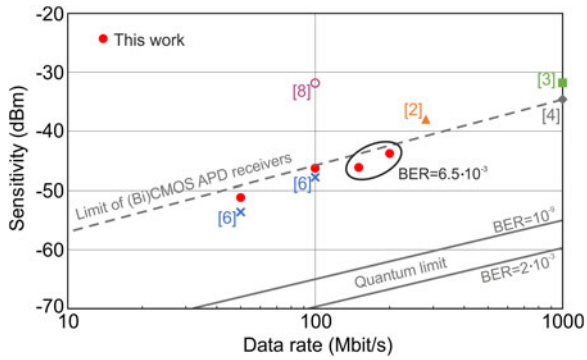

Fig. 9. Comparison of the sensitivities for the state of the art.

for a BER of 10^{-9} and $2\cdot10^{-3}$ is also included within Fig. 9. The new sensitivities at 50 Mbit/s and 100 Mbit/s are a little bit worse compared to [6] because of the shorter dead time and the higher APP. The smaller light sensitive area of the SPADs in the new receiver could not compensate this. As it can be seen the sensitivities for 50 Mbit/s and 100 Mbit/s are still better than the limit given by linear mode OEICs and the maximal data rate was improved by a factor of two compared to [6].

V. CONCLUSION

This work reports the first SPAD based receiver with an integrated processing circuit for data rates up to 200 Mbit/s. This high data rate was realized using an array of 4 SPADs and a reduced dead time of 3.5 ns for the active quenching circuits. Due to the short dead time, parasitic effects are increased. Especially the afterpulsing probability limits the performance of the reported receiver. The best extracted sensitivities for 50 Mbit/s and 100 Mbit/s are at −51.1 dBm and −48.4 dBm, respectively (at a BER of $2\cdot10^{-3}$) and are still better than the limit given from linear-mode APD OEICs.

The integrated post processing circuit is working very well up to data rates of 100 Mbit/s. For higher data rates the results leave room for improvement. First, an additional 3 out of 4 output would give a better BER characteristic for data rates higher than 100 Mbit/s. Second, the time of 1.5 ns needed for the read out of the circuit and making the receiver insensitive for this time additionally limits the BER.

The presented sensitivities for 150 Mbit/s and 200 Mbit/s of −46.1 dBm and −43.8 dBm were extracted with MATLAB latch-type processing of the CQC outputs.

Including an additional 3 out of 4 output and further optimization of the dead time and of the timing parameters of the integrated processing circuit will help to further decrease the gap towards the quantum limit even for higher data rates.

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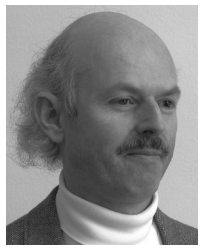

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