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Bernhard Steindl
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Optimized silicon CMOS reach-through avalanche photodiode with 2.3-GHz bandwidth

Bernhard Steindl,* Tomislav Jukić, and Horst Zimmermann
Vienna University of Technology, Institute of Electrodynamics, Microwave and Circuit Engineering, Vienna, Austria

Abstract. Optimizing avalanche photodiodes (APDs) in standard complementary metal–oxide–semiconductor (CMOS) processes is challenging due to fixed doping concentrations of the available wells. A speed-improved APD in pin photodiode CMOS technology for high-sensitivity and high-speed applications using a lateral well modulation-doping technique is presented. The increased operating voltage of the presented device leads to a −3-dB bandwidth of 2.30 GHz with a multiplication factor of 20 for 1-μW optical power. This corresponds to a responsivity of 7.40 A/W. A multiplication factor of 44,500 was measured at 10-nW optical power. The thick absorption zone leads to an unamplified quantum efficiency of 72.2% at 635-nm wavelength. © *2017 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.OE.56.11.110501]

Keywords: avalanche photodiodes; optoelectronic integrated circuits; photodetectors.

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1 Introduction

Utilizing the internal amplification of linear-mode avalanche photodiodes (APDs), optical receivers with integrated APDs instead of standard pin photodiodes are interesting for high-sensitivity applications. Such applications are optical data transmission via plastic optical fiber or optical free-space communication and biomedical medical imaging for continuous wave near-infrared spectroscopy.[1–3] Compared to common pin photodiodes, APDs show an internal avalanche gain with the so-called multiplication factor M. To meet the requirements of high-speed data communication, APDs require high quantum efficiency as well as a high bandwidth. Using an APD in a combined optical integrated receiver chip (optoelectronic integrated circuit) fabricated in a Si complementary metal–oxide–semiconductor (CMOS) process reduces the influences of parasitic effects and furthermore allows a cost-effective production.

The multiplication process of an APD is based on the impact ionization effect. This effect occurs above a certain energy of the accelerated photogenerated carriers. Two general design concepts for Si CMOS APDs were reported in the literature.[3–8]

Si CMOS APDs based on n^+/p-well and p^+/n-well structures were reported in Refs. 3–5. The responsivity of those devices is generally limited due to the rather thin depleted absorption zone defined by the thickness of the well structure. The penetration depth of photons in silicon increases with the wavelength. The carriers generated underneath the well in the APD structure do not contribute to the output current. The usual thickness of the absorption zone (predefined by the well structure), therefore, reduces the spectral quantum efficiency and the spectral responsivity (R) on one hand but increases the bandwidth on the other hand. The maximum responsivities of the APDs reported in Ref. 4 for a wavelength of 850 nm are 4.30 A/W ($M = 493$) and 3.52 A/W ($M = 417$). The maximum bandwidth was 3.4 GHz with $R < 0.2$ A/W.[4] For 850 nm, the maximum responsivity reported in Ref. 5 is 10 A/W ($M = 1993$) with maximum bandwidth of 3.2 GHz for $R = 2.94$ A/W.

A so-called reach-through design concept using standard CMOS processes is reported in Refs. 6–8. These APDs consist of an additional separate thick absorption zone and the multiplication zone located at the interface of the n^+-cathode doping region and the p-well. The epitaxial layer fully depleted at a reverse bias voltage of 19 V while the breakdown occurred at 35.25 V.[8] This device showed a high unamplified responsivity of 0.31 A/W at 670-nm wavelength and a bandwidth of 1.02 GHz ($M = 61.4$) limited by carrier drift in the thick absorption zone.[8]

Due to the limitations of the fixed doping profiles in standard CMOS, optimizations of the APD design are usually a major challenge. This letter presents a speed-improved APD using the lateral well modulation-doping technique reported in Ref. 9 for a standard digital CMOS process, where no low-doped epitaxial layer was present and bandwidths of up to 386 MHz were achieved for the maximum possible reverse voltage of the integrated APD. The technique reported in Ref. 9 suggested different design patterns (dots, stripes, and holes) to manipulate the effective doping concentration of the well structure. The basic APD concept presented in this letter was previously reported in Ref. 8. The modulation technique[9] uses only layout techniques, i.e., it does not require process modifications, and can be, therefore, easily used to expand the depletion edge (space-charge region) down to the substrate or to increase the electrical field strength in the absorption zone for a reduced drift time of the photogenerated carriers. The doping concentration of the modulated p-well for the presented APD was reduced by a factor of 0.83 using the hole pattern structure demonstrated in Fig. 1. Without any process modifications, this reduction leads to an increased bandwidth of 2.30 GHz at a multiplication factor of 20 ($R = 7.4$ A/W at 635 nm). Since the minimum ripple of the hole pattern is at a doping factor of ~80%,[9] the device with a doping factor of 83% can be considered as speed optimized at the minimum modulation ripple.

2 Avalanche Photodiode Structure

The APD has a circular shape with an active diameter of 90 μm and was fabricated in a 0.35-μm pin photodiode CMOS process. Figure 1 contains the general structure of

*Address all correspondence to: Bernhard Steindl, E-mail: bernhard.steindl@tuwien.ac.at

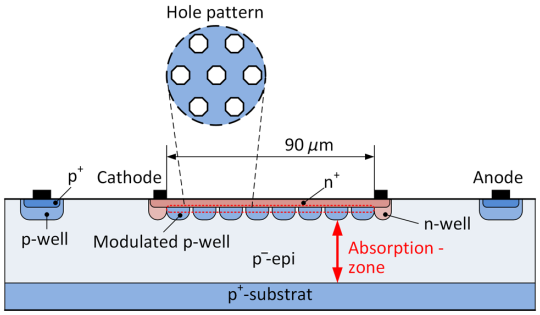

Fig. 1 Cross section of modulation-doped APD and the hole pattern structure of the p-well's layout (not to scale).

this device. The APD consists of a separate absorption and multiplication zone. The incoming photons are absorbed inside the thick p^--epitaxial layer (p^--epi). The thickness of this layer with a doping concentration of about 2×10^{13} cm^{-3} is ~12 μm. The multiplication takes place at the interface between the modulated p-well and the n^+-cathode area. For this APD, the effective p-well doping was reduced by a factor of 0.83. In the case of reverse biasing of the APD, the photogenerated electrons inside the absorption zone are accelerated toward the multiplication zone. Due to impact ionization, the number of carriers is multiplied by the factor M and collected at the cathode. An additional n-well at the boundary of the n^+ region was used to avoid lateral edge breakdown. Within the layout, the p-well was laterally modulation doped using the technique reported in Ref. 9 applying a so-called hole pattern (see Fig. 1). In the end, an almost homogenous doping concentration results due to dopant diffusion and the thermal budget of the used CMOS process suggesting a low excess noise factor of this APD, which is supported by the sensitivity of −31.8 dBm at 1 Gbit/s (BER = 10^{-9}) of a receiver containing the modulation-doped APD with a diameter of 600 μm.[10]

3 Experiments

Controlling the doping concentration of the p-well leads to a more or less adjustable breakdown voltage (V_{BD}) for this APD. M strongly depends on the bias voltage. In contrast to the original device, the multiplication factor of the modulated device decreases when compared with identical reverse bias voltages. Figure 2 shows the reverse voltage characteristics of the dark current and the photocurrent at different optical input powers (−50, −40, and −30 dBm) of the modulation-doped device. These measurements were done with a 635-nm laser source having an internal monitoring diode and an adjustable optical attenuator. The current is measured with a Keysight B2987A electrometer, and the temperature of the device under test is regulated to 25°C. Compared to the original APD reported in Ref. 8 (V_{BD} = 35.25 V), the breakdown voltage of the modulated device is increased by a factor of 1.52 to ~53.7 V. The unamplified responsivity is 0.37 A/W at 635 nm, which corresponds to a quantum efficiency of 72.2% at this wavelength. The responsivity is slightly different compared to the original device at 635 nm (0.33 A/W[8]), due to variations of the thickness of oxide stack, since no opto-window and therefore no antireflection coating was available for the used APD structure. For 850 nm, a responsivity of 0.29 A/W can be estimated from Fig. 3 in Ref. 8.

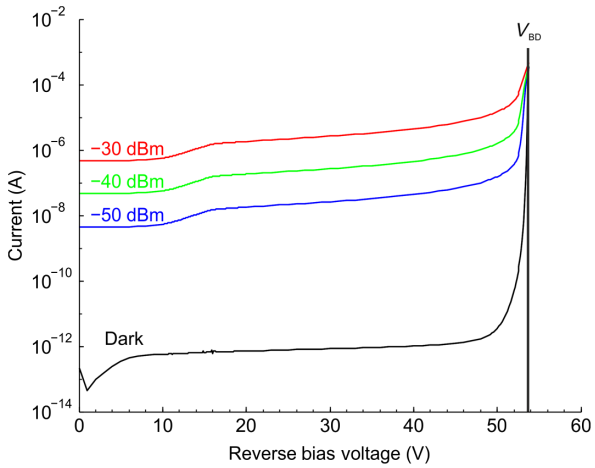

Fig. 2 Dark and photocurrent versus reverse bias voltage at −50-, −40-, and −30-dBm optical power.

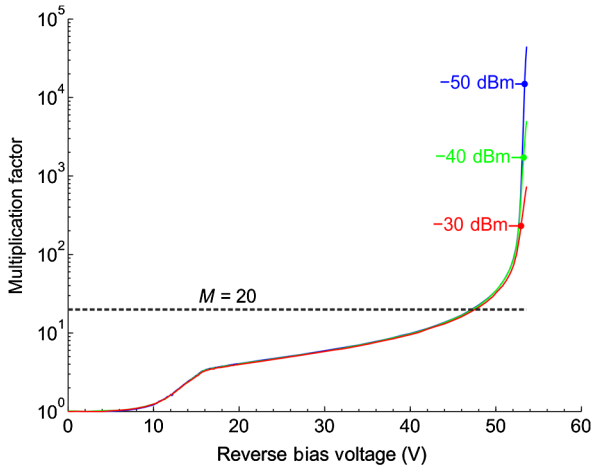

Fig. 3 Multiplication factor versus reverse bias voltage at −50-, −40-, and −30-dBm optical power.

Figure 3 contains the calculated multiplication factor for all three optical input powers (the dark current was subtracted). As can be seen, the curves are overlapping over a broad voltage range. Above 52 V (M = 70), the multiplication factor increases rapidly for increasing reverse voltage V_B. However, with increasing optical power, the slope is smaller due to saturation effects of the multiplication process.[11] A multiplication factor of 20 is achieved at 47.5 V, independent of the optical illumination power. At 53.6 V, for an optical power of −30 dBm (1 μW), the multiplication factor is ~730, for −40 dBm (100 nW), the multiplication factor is 5000, and for −50 dBm (10 nW), it is 44,500. Table 1 shows an overview of the corresponding responsivities.

The frequency response of the APD was measured for different multiplication factors at an optical power of −30 dBm using a Rohde & Schwarz ZVM20 vector network analyzer. For easier comparison, the curves in Fig. 4 were normalized at the frequency of 1 MHz. Below 1 GHz, the responses for M = 8 and M = 20 are almost congruent. The maximum −3-dB bandwidth of 2.30 GHz was measured at M = 20 (V_B = 47.5 V). As mentioned before, a higher bias voltage leads to a reduced drift time of the photogenerated carriers in

Table 1 Overview of the corresponding responsivities at 635-nm wavelengths.

Optical power (dBm)	Reverse bias voltage	Multiplication factor	Responsivity (A/W)
−50	53.6	44,500	16,465
−40	53.6	5000	1850
−30	53.6	730	270.1
−30	52.2	80	29.6
−50, −40, −30	47.5	20	7.40
−50, −40, −30	37.0	8	2.96

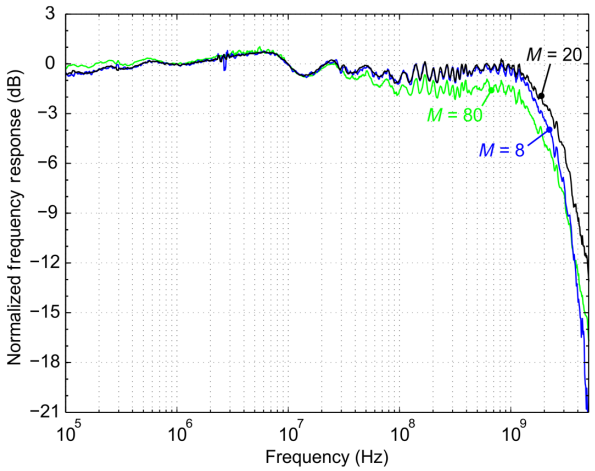

Fig. 4 Normalized frequency response at −30-dBm optical power for multiplication factors of 8, 20, and 80.

the absorption zone. For a lower multiplication factor, the electric field strength, and therefore the reverse voltage, has to be reduced in the multiplication zone. However, then also the electric field strength in the absorption zone becomes lower, leading to a lower bandwidth of 1.92 GHz for $M = 8$ ($V_B = 37.0$ V). In general, the avalanche process needs additional time (avalanche build-up time). A high multiplication factor increases the avalanche build-up time and therefore limits the bandwidth. This effect can be clearly seen in Fig. 4 for $M = 80$ ($R = 29.6$ A/W, $V_B = 52.2$ V). The resulting bandwidth of 1.48 GHz, however, is still 1.45 times higher than the maximum bandwidth reported in Ref. 8.

4 Conclusion

Thin APD structures increase the bandwidth by reducing the thickness of the absorption zone to minimize the traveling time of the generated carriers. This leads to a limited unamplified responsivity for those device structures (0.0085[4] and 0.0052 A/W[5]) compared to the estimated responsivity of 0.29 A/W at 850 nm for the presented APD.

The optimization of the bandwidth for the presented APD using a thick absorption zone was done by reducing the effective p-well doping without any drawbacks regarding the unamplified responsivity (0.37 A/W at 650 nm). The presented APD shows a maximum bandwidth of 2.3 GHz at a multiplication factor of 20 ($R = 7.4$ A/W) and a bandwidth of 1.48 GHz at $M = 80$ ($R = 29.6$ A/W). This is an improvement by factors of 2.25 and 1.45, respectively, compared to the maximum bandwidth (1.02 GHz at $R = 19$ A/W) of the unmodulated device reported in Ref. 8.

Acknowledgments

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