Fully integrated optical receiver using single-photon avalanche diodes in high-voltage CMOS

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Abstract. A monolithic optical receiver containing four single-photon avalanche diodes (SPADs) fabricated in 0.35-μm high-voltage (HV) CMOS is introduced and compared with two 4-SPAD receivers realized in pin-photodiode CMOS belonging to the same process family. This HV-CMOS SPAD receiver achieves sensitivities of −55.1 dBm at 50 Mbit/s and −52.0 dBm at 100 Mbit/s, both with digital processing, a bit error rate (BER) of 2×10^{-3}, and return-to-zero coding using a wavelength of 642 nm. Also at 143 Mbit/s, this BER is achievable. This receiver is especially interesting for applications in which low light intensities can be expected, such as quantum key distribution, optical communications from deep space, and visible light communication for short-range consumer applications. © *2020 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.OE.59.7.070502]

Keywords: optical receiver; single-photon avalanche diode; quantum limit; optoelectronic integrated circuits.

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1 Introduction

With the use of avalanche photodiodes (APDs) in optical receivers, the sensitivity has been improved stepwise in recent years. Due to the excess noise of APDs and electronic noise of transimpedance amplifiers, however, a gap of about 20 dB to the quantum limit for bit error rate $(\mathrm{BER}) = 10^{-9}$ still exists for linear-mode APD receivers.[1–7] Utilizing pulse-position modulation (PPM), the sensitivity of APD receivers can be increased by encoding M bits into each laser pulse by transmitting the pulse at one of 2^M positions within a defined symbol frame. In Ref. 8, Sun and Davidson show a BER of 10^{-6} for less than 60 detected photons at 25 Mbit/s using linear mode APDs. Because the photon rate in Ref. 8 only accounts for detected photons, the actual photon rate needs to be higher due to losses and nonidealities, such as the quantum efficiency of the APDs. Biswas et al. achieved a sensitivity of 11 to 12 photons/bit at a relatively high BER of 10^{-2} and a low pulse rate of 50 to 100 K pulses per second with 8 bits per pulse (i.e., corresponding to data rates between 400 and 800 Kbit/s).[9]

With APDs in the Geiger mode, i.e., with so-called single-photon avalanche diodes (SPADs), the sensitivity of optical receivers can be further improved because the very high internal amplification eliminates the impact of excess noise and electronic noise. However, parasitic effects of SPADs limit the achievable sensitivity. The first integrated SPAD-based optical receivers were published by Fisher et al.[10] and Chitnis and Collins.[11] In Ref. 10, a 32×32 SPAD-array was used to reach a sensitivity of −31.7 dBm at 100 Mbit/s, a BER of 10^{-9}, and a 450 nm wavelength. The main goal of this receiver was to obtain a large dynamic range of 79 dB. An array of 100 SPADs was exploited in Ref. 11 at 20 Mbit/s; however, no sensitivity was reported. An SPAD receiver in 0.13-μm CMOS was reported in 2015 by Almer et al.,[12] in which a pulse amplitude modulation technique (4-PAM) was used to achieve a sensitivity of −64 dBm at 100 kbit/s with a 32×32 SPAD array. For a data rate of 1 kbit/s and an array of 1024 SPADs with an orthogonal frequency multiplex method, a sensitivity of −107 dBm at 1 kbit/s was reported by Li et al.[13] Goll et al. introduced a one-SPAD receiver in 2018 with a cascoded gating circuit in 0.35 μm CMOS.[14] The SPAD had a diameter of 50 μm, and the circuit enabled five sub-bits. At 20 and 50 Mbit/s, sensitivities of −64 and −57 dBm, respectively, were achieved ($\mathrm{BER} = 2 \times 10^{-3}$).

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An SPAD receiver with 64×64 elements realized in 130-nm CMOS was published by Kosman et al.[15] For a BER $= 2 \times 10^{-3}$, a wavelength of 450 nm, and 4-PAM enabling a data rate of 500 Mbit/s, a sensitivity of -46.1 dBm was reached.

PPM was also used with SPAD receivers. Yarnall et al. presented laser communication using a 32×32 SPAD array and a 16-ary PPM. A BER of 10^{-1} was achieved with only 0.8 detected photons per bit at a data rate of 38.8 Mbit/s. Losses, e.g., due to the nonideal photon detection probability (PDP), are not included.[16] In Ref. 17, Lu et al. mitigated the effects of afterpulsing and dark counts by either utilizing coincidence measurements between two detector arrays or using a two photon threshold, both with a silicon photomultiplier that allows for counting the number of photons. Data rates of up to 100 and 400 Mbit/s were achieved with two photon threshold and coincidence measurement, respectively. No dedicated value for the sensitivity was given. However, extracted from the BER characteristic, a sensitivity of $\approx$10 photons/bit can be estimated at a BER of 10^{-3} for 100 Mbit/s. But it is unclear if this photon rate is the detected photon rate or the real one.

Because large arrays of SPADs may suffer from dark counts and optical crosstalk, 4-SPAD receivers were investigated. Sensitivities of -55.7 and -51.6 dBm (BER $= 2 \times 10^{-3}$, dead time 9 ns) at 50 and 100 Mbit/s, respectively, were achieved with red light (635 nm) due to a thick absorption zone in 0.35-μm pin-photodiode CMOS.[18] A 4-SPAD receiver with a dead time of only 3.5 ns and on-chip digital processing in the same 0.35-μm technology achieved data rates of 150 and 200 Mbit/s at sensitivities of -46.2 and -43.8 dBm, respectively, with a BER of 6.5×10^{-3} for which error correction is also possible with a slightly larger overhead.[19,20] In 0.35-μm high-voltage (HV) CMOS, however, an SPAD with a thick absorption zone also was investigated. This HV-CMOS SPAD was fabricated with an antireflection coating on top and showed a PDP of about 45% at 635 nm and 6.6 V excess bias V_{ex}.[21] Therefore, a 4-SPAD receiver in 0.35-μm HV CMOS was designed and fabricated to compare with the 4-SPAD receivers in pin-photodiode CMOS. The results of the 4-SPAD HV CMOS receiver are presented in this letter.

2 Receiver Structure

The core of the receiver presented in this letter consists of an array with 4-SPAD elements connected to cascoded quenching circuits (QC). The block diagram is shown in Fig. 1. The used QC with a low detection threshold is similar to the QC that was described in detail in Ref. 18. The cascoded structure of this circuit allows for a maximal excess bias voltage of 6.6 V and an adjustable dead time between 5.8 and 34 ns. The output stage of each of the four channels is formed by a 50-Ω buffer.

The microphotograph of the implemented test chip is shown in Fig. 2. Additional circuits were integrated on this receiver chip but are not used and not considered in this work. The total size of the chip is 1160×2120 μm^2, whereby the most important blocks, consisting of the SPAD array, the QCs, and the output drivers, are highlighted in the figure. In the idle state (no detection), the average power consumption of all QCs over the entire dead time is $\sim$24.4 mW. The simultaneous detection of a photon in each of the four SPADs increases the total power consumption to 40.4 mW.

The used array consists of four circular SPAD elements. The active area of each SPAD is about 5000 μm^2. The SPAD-array was illuminated by means of a single-mode fiber, and the

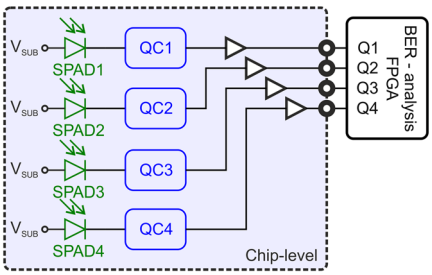

Fig. 1 Block diagram of the receiver.

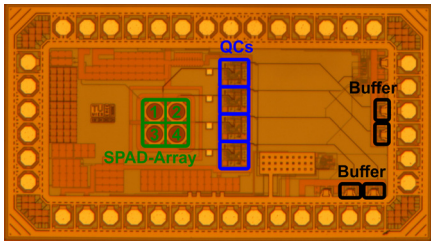

Fig. 2 Microphotograph of the 4-SPAD-receiver. The main parts are highlighted (SPAD-array, QCs, and buffers).

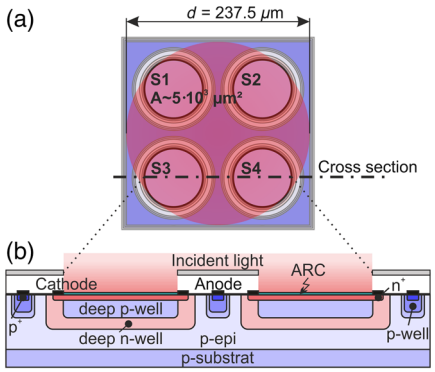

Fig. 3 (a) Layout of the SPAD-array and (b) cross section (not to scale).

distance of the fiber to the chip surface was optimized to maximize the amount of light received by the SPADs. Assuming a Gaussian distribution of the photons in the light spot, this results in an effective fill factor of 37.7%, i.e., this fraction of the photons in the Gaussian distributed light spot is seen by the four SPADs in total.

The layout of the array and the cross section of the SPAD-elements are presented in Fig. 3. Each SPAD consists of a highly doped n+ cathode. The multiplication zone is formed at the interface between the n+ and the deep p-well. The surrounding deep n-well reduces the effective doping concentration inside the deep p-well and additionally prevents edge breakdown effects. The p-epi layer is used as the absorption zone. The dark count rate (DCR), afterpulsing probability (APP), and PDP of this SPAD structure were characterized in a previous publication.[22] The best sample in this paper achieves a DCR of 41.7 kcps, an APP of 57.6%, and a PDP of 43.6% at a 642 nm wavelength (all values at dead time $t_d = 5.8$ ns and excess bias $V_{ex} = 6.6$ V).

Parasitic avalanche events such as DCR, APP, and optical crosstalk probability (OCTP) limit the achievable sensitivity of the receiver. Therefore, we measured the performance of each segment. For this measurement, we adjusted a medial dead time of 8.9 ns.

The breakdown voltages (V_{bd}) for the SPADs in this array differ by 0.4 V. SPAD 1 (S1) has the lowest V_{bd} of 70.7 V. The elements show a similar DCR (82.2 kcps for SPAD 3 at $V_{ex} = 6.6$ V) and an APP between 35% and 40% at $V_{ex} = 6.6$ V. In the worst case, at $V_{ex} = 6.6$ V, the OCTP between two direct neighboring SPADs is in average 5.3%. The diagonal crosstalk is about 1.8%. In addition, the crosstalk for three segments was only measured above $V_{ex} = 4.6$ V (0.3% at $V_{ex} = 6.6$ V). The optical crosstalk for all four elements was not registered in the specified voltage range for a measurement time of 1 s. In particular, the APP of SPADs depends on the dead time of the QC. As shown in Ref. 22, by increasing the dead time, the achievable APP decreases dramatically.

3 Experimental Results

For the evaluation of the BER for this 4-SPAD receiver, we developed a real-time characterization system. This system includes the generation of the modulation signal for the laser source

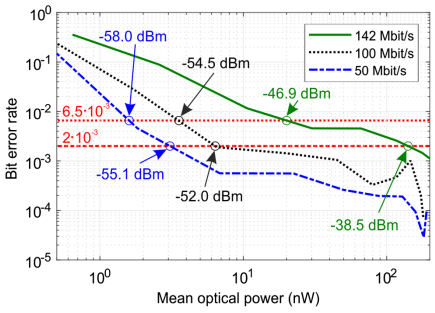

Fig. 4 BER versus mean optical power.

(wavelength $\lambda = 642$ nm) and a digital processing method for the BER extraction. As shown in Fig. 1, all four output signals of the QCs are added digitally at a defined sampling time in an FPGA. The final sampling values are then determined with a decision threshold (one out of four to four out of four) and compared internally in the FPGA with the original modulation signal. After the optimal alignment of the optical fiber, the BER was determined at data rates of 50, 100, and 143 Mbit/s by varying the mean optical power and the excess bias voltage V_{ex}.

The modulation signal for the laser source is also generated in the FPGA to be able to easily compare received data with sent data. Due to a clock rate of the system of 1 GHz after the serializer, only data signals with a duration of an integer multiple of 1 ns can be generated. A bit duration of 7-ns results in a data rate of 142.86 Mbit/s (143 Mbit/s). For the modulation signal (a pseudorandom bit sequence PRBS-7), binary return-to-zero (RZ) coding with a laser duty cycle of 30% was used for 50 and 100 Mbit/s. At 143 Mbit/s, a duty cycle of 43% (3 ns) was used. The extracted BER curves of the SPAD receiver are summarized in Fig. 4.

The dead time t_D was adapted to the different data rates to roughly correspond to the time difference between the falling edge of the RZ signal and the rising edge of the next bit. This results in $t_D = 14$ ns for 50 Mbit/s and $t_D = 7$ ns for 100 Mbit/s. The minimum dead time of 5.8 ns was used for 143 Mbit/s.

The results in Fig. 4 clearly show that the critical threshold for forward error correction (FEC) of a BER $= 2 \times 10^{-3}$ was undershot for all three data rates. The best results at these data rates were achieved with a decision threshold of three out of four. The extracted sensitivity was -55.1 dBm (3.1 nW) for 50 Mbit/s. As mentioned above, the BER for this receiver was also examined at 100 Mbit/s and 143 Mbit/s. At 100 Mbit/s, the sensitivity is -52.0 dBm (6.4 nW) at a BER of 2×10^{-3}. For 143 Mbit/s, it is -38.5 dBm (140.8 nW). For a BER of 6.5×10^{-3} the sensitivities are -58.0 dBm (1.6 nW), -54.5 dBm (3.5 nW), and -46.9 dBm (20.3 nW) for 50, 100, and 143 Mbit/s, respectively. For this higher BER, FEC is still feasible but requires more overhead.

4 Discussion

To achieve correctable BERs despite the parasitic avalanche events of the SPADs, whereby APP and OCTP dominate, the suggested receiver contains an array of four SPADs. Other than the Poisson distribution of the photons, the sensitivity is mainly limited by the fill factor, the decision threshold, and the PDP of the SPADs. For the geometry used, the fill factor is 37.7%, resulting in a loss of 4.2 dB. The decision threshold, which requires that at least three of the four SPADs need to detect a photon, adds another 4.2 dB to the gap to the quantum limit, assuming Poisson distribution of the photons. The remaining gap to the quantum limit is mainly caused by the limited PDP. While these SPADs achieve PDPs of up to 43.6% for $V_{\mathrm{ex}} = 6.6$ V, such a large excess bias voltage would result in a too large BER because the APP also increases with increasing excess bias voltage. The remaining gap to the quantum limit after subtracting the influence of the fill factor and the decision threshold corresponds to the effective PDP of the SPADs in the bias point when the BER of 2×10^{-3} is reached. This effective PDP is 9.5%, 9.3%, and 1.2% for 50, 100, and 143 Mbit/s, respectively. Increasing the effective PDP is possible by increasing the number of elements in the SPAD array and increasing the decision threshold (i.e., the minimum number

of SPADs that have to detect a photon during a bit to receive a digital "1") or by increasing the dead time. With an increased decision threshold, the influence of the APP decreases.[15] However, increasing the decision threshold will also increase the loss caused by it. An increased dead time directly decreases the APP but limits the achievable data rate.

In Ref. 18, the best sensitivities were obtained with analog processing of the quencher output signals (i.e., −55.7 and −51.6 dBm at 50 and 100 Mbit/s, respectively, at a BER $= 2 \times 10^{-3}$ and dead time $t_D = 9$ ns). This analog approach used a filter that was optimized for each data rate. With digital processing of the quencher output signals, the sensitivity in RZ (BER $= 2 \times 10^{-3}$) at 100 Mbit/s was −47.8 dBm in Ref. 18 and −46.3 dBm in Ref. 20. Compared with the digital processing approaches with the SPAD receivers in pin-photodiode CMOS of Refs. 18 and 20, the receiver presented here achieves a considerable improvement of the sensitivity to −52.0 dBm at 100 Mbit/s (BER $= 2 \times 10^{-3}$). A BER of 2×10^{-3} was not possible at 150 Mbit/s in Ref. 20, whereas the presented HV CMOS SPAD receiver achieves this BER at 143 Mbit/s.

One big advantage of the SPADs in the presented HV CMOS receiver is that these SPADs have an opto-window with an antireflective coating, whereas the SPADs in the pin-photodiode receiver do not. Without an opto-window, interference effects within the oxide stack can lead to increased reflection and therefore to increased loss of received light, depending on the wavelength. The spectral PDP therefore shows "oscillations." This is not the case when using an opto-window. The advantage of the pin-photodiode CMOS process is the low-doped epitaxial layer that has a doping much lower than the one in HV CMOS. Due to this lower doping, a thick depletion zone is possible with lower voltages compared with the HV CMOS process. Because of this, the operating voltage in the HV CMOS process needs to be higher if a thick depletion zone is required, which is, e.g., needed if the wavelength to be detected is in the infrared range. However, the high voltage transistors in HV CMOS potentially allow for implementing quenchers with even higher excess bias voltages, resulting in a higher PDP.

5 Conclusion

The results obtained show that the high PDP for the red light of SPADs in a standard HV CMOS technology without any process modifications enables a data receiver with better sensitivities than two other receivers in pin-photodiode CMOS using comparable digital processing. The presented 4-SPAD receiver in an inexpensive sub-μm CMOS technology can be used for up to 143 Mbit/s with a BER even below 2×10^{-3}, enabling effective FEC. For the HV CMOS SPAD receiver described here, the distances to the QL for a BER $= 2 \times 10^{-3}$ at 50 and 100 Mbit/s are 18.7 and 18.8 dB, respectively (the QL is −73.7 and −70.7 dBm for 50 and 100 Mbit/s, respectively).

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