Fully Integrated Actively Quenched SPAD in 0.18µm CMOS Technology

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***Abstract*—A fully integrated single- photon avalanche diode (SPAD) in a 180 nm high voltage CMOS technology is presented. The introduced quenching circuit is realized by the 3.3V high voltage transistors of the process to increase the excess bias voltage V_{ex} above the usual 1.8V supply voltage of the 180nm CMOS technology. Furthermore the circuit is cascoded to increase the excess bias even more up to 6.6V.**

Keywords—SPAD, optical receiver, CMOS, active quenching

I. INTRODUCTION

The idea to detect less and less optical power drives the development of optical sensors and receivers towards the use of single-photon avalanche diodes (SPADs). These detectors are able to detect single photons hitting the active area. To achieve this, avalanche photodiodes (APDs) are biased in the so called Geiger mode. The bias voltage of the APD is increased beyond the breakdown voltage (V_{BR}) and as soon as a photon hits, the breakdown happens, an avalanche of charge carriers is built up and the subsequent voltage drop across the diode quenches the bias voltage below V_{BR} and therefore the avalanche is pinched off.

There are different types of quenching circuits (QCs), passive ones and active QCs. The simplest passive quencher consists of a resistor. This circuit has the disadvantage that the quenching time is rather long and the following reset time until the bias voltage (V_{bias}) is again set above V_{BR} is even longer. V_{bias} is defined by V_{BR} and the excess voltage V_{EX} ($V_{bias} = V_{BR} + V_{EX}$). To increase the speed of a quenching cycle, active quenchers detect the voltage drop across the resistor, decrease V_{bias} rapidly below V_{BR} and set it back to $V_{BR} + V_{EX}$ after the avalanche is quenched. Obviously the SPAD detector is not able to detect another photon during the quenching cycle. The time between hit of the photon and the next possible detection is called dead time (t_D).

II. CHARACTERISTICS OF SPADS

Typical characteristics of SPADs are the dark count rate (DCR), the afterpulsing probability (APP) and the photon-detection probability (PDP).

A. Dark Count Rate and Afterpulsing Propability

The DCR defines the amount of counts not induced by a photon. These pulses can be generated either by uncorrelated interactions (e.g. thermally induced) between charge carriers and lattice defects of the semiconductor, so called charge traps, as described in [1], or correlated pulses which occur after a pulse. So called deep level traps are filled during the main avalanche of a pulse and after a statistical delay released carriers generate a secondary avalanche and therefore an afterpulse [2]. The lifetime of these carriers is in the nanosecond range and therefore the afterpulsing probability (APP) is directly correlated to the dead time of the QCs.

B. Photon Detection Probability

The quantum efficiency η describes the probability of generating an electron-hole pair out of a photon.

$$\eta = \frac{N_e}{N_p} = \frac{I_{ph}}{q \cdot \Phi} \tag{1}$$

where N_e describes the photo-generated electrons and I_{ph} the photocurrent. N_p is the number of incoming photons, Φ is the photon flux, and q the elementary charge.

For single-photon detectors, normally the PDP is used instead of the quantum efficiency. Analogous it is calculated by

$$PDP(\lambda) = \frac{N_d}{N_p(\lambda)} \tag{2}$$

with N_d is the number of detected photons and N_p the amount of incoming photons. Since the responsivity of the diode depends on the wavelength (λ), also the PDP depends on it. Other reasons for a PDP <1 are e.g. the photon is absorbed outside of the active area, it might be reflected on the detector surface, the photon transmits, it is absorbed in the active area, but is not detected due to recombination or other parasitic effects, or no self-sustaining avalanche happens.

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III. Integration of the SPAD

The SPAD is integrated in a high voltage 180 nm CMOS process.

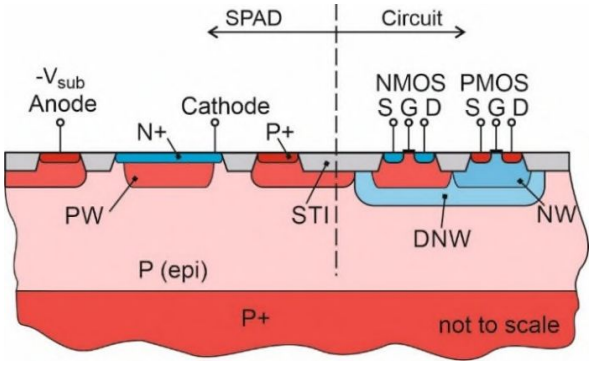

Fig. 1. Cross section of SPAD and concept of isolated transistors

The anode of the SPAD is directly connected to the substrate of the microchip, see Fig. 1, and therefore the QC has to be isolated from the substrate, due to a V_{BR} above the supply voltage of the circuit. The circuit is completely surrounded by deep N-wells (DNW) to ensure the isolation towards the substrate. The technology offers an isolation of 40 V between the substrate and the DNW.

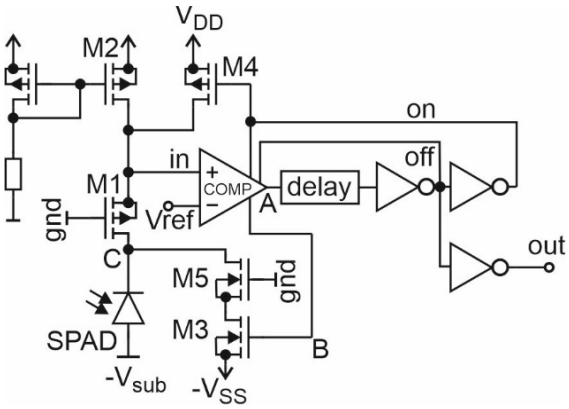

Fig. 2. Overview schematic of cascoded active quenching circuit

The SPAD cathode is connected to the QC, the multiplication zone is between the N+ and the P-well (PW), the absorption zone is in the PW and in the P-epi area. The P-epi of this process is higher doped compared to the opto-process reported in [3] and therefore the absorption zone is thinner, because the epi-layer is not fully depleted at the breakdown and excess bias voltage.

The diameter of the active area of the circular SPAD is 16 µm, while the complete SPAD occupies 1964 µm².

IV. Quenching Circuit

The QC is designed as cascoded active quencher. The schematic of the circuit is depicted in Fig. 2.

Node C is the cathode of the SPAD, which is close to V_{DD} when it is biased in Geiger mode, before a photon hits.

$$|V_{DD}| + |V_{sub}| = |V_{BR}| + |V_{EX}| \qquad (3)$$

The negative substrate voltage V_{sub} delivers the necessary bias voltage according to .

As soon as an event occurs, an avalanche is built up and the current through M2 leads to passive quenching (M4 is off), which reduces the gate-source voltage of M1 and therefore the input voltage of the comparator (COMP) (and also V_C, see Fig. 4). As soon as it reaches V_{ref} = 3.2V, after 0.25 ns,he in Fig. 3 detects the event, V_A turns to "high" and turns off the pre-bias of V_B and it is pulled to "high" as well, but in the lower voltage regime, between ground and -V_{SS}. V_B is pre-biased to get a fast response time (see Fig. 5).

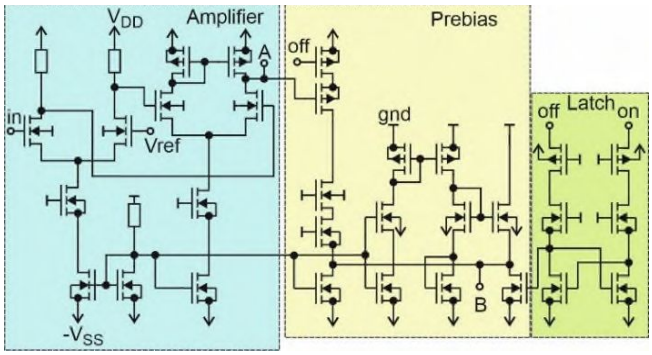

Fig. 3. Schematic of COMP

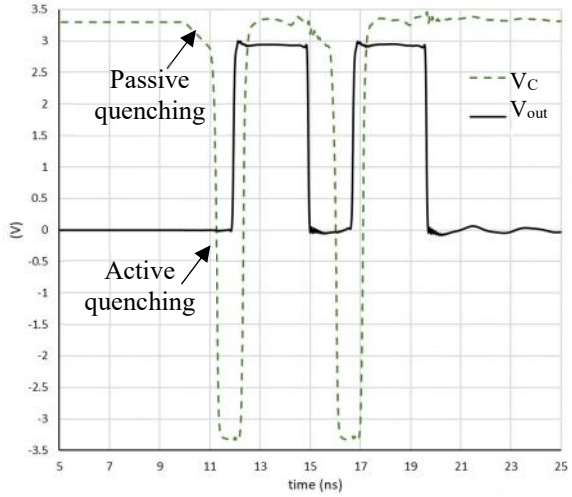

Fig. 4. Transient voltages (postlayout simulation), minimum dead time

Then, M3 (Fig. 2) is turned on, which decreases V_C rapidly, in 0.34 ns, to -V_{SS}, and therefore below V_{BR}, consequently, the avalanche is quenched. The overall quenching time betweenandis 1.34 ns. Fig. 5 depicts the transient voltages of the described nodes for the maximum dead time. In the meantime, the voltage at node A (V_A) starts the reset again. Via the delay block and the following inverters the dead time is variable. The voltage at node "on" (V_{on}) equals V_{DD}, except for the reset pulse close to the end of the deadtime, generated by the latch (Fig. 1) when the voltage of node B (V_B) is reset to -V_{SS} again and V_C is pulled back towards V_{DD} by M4. The transistors M1 and M5, as well as the cascode transistors in the COMP, are necessary to keep all transistors in the save operating area. The COMP works similar to the active quenching circuit in-depth described in [3], which was realized in a 0.35µm CMOS process with a thick low doped p-epi layer. All transistors are high-voltage transistors which enable a supply voltage of 3.3 V and due to the cascoded concept the total voltage swing is 6.6 V.

The circuit offers dead times from 4.5 ns (Fig. 4) to more than 30 ns (Fig. 5) but unfortunately the APP of the diode is

rather high and the measurement results were best for the maximum dead time.

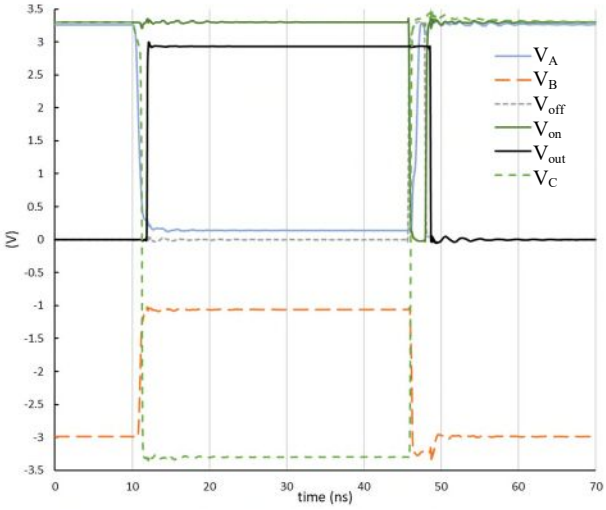

Fig. 5. Transient voltages (post layout simulation) for maximum dead time

Fig. 1 shows the microphotograph and a layout plot of the circuit. The active area of the quenching circuit inclusive SPAD is 185 µm × 150 µm.

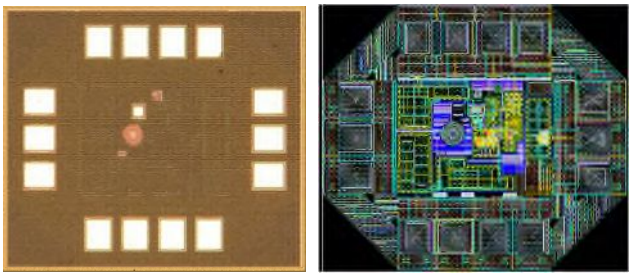

Fig. 6. Microphotograph and layout plot of the chip

V. Measurement Setup

The device under test (DUT) was bonded onto a printed circuit board (PCB), which is mounted on a copper block for temperature stabilization. A temperature sensor placed within the copper block as well as a thermo-electric cooler are used to stabilize the DUT's temperature at 25°C. For the measurement, the DUT is placed in a dark box to remove all background light. Inside this dark box, also the detector of a Thorlabs power meter (PM200) and a motorized xyz stage are placed. For the PDP measurements, the laser light is guided to the DUT using a SM600 single-mode fiber. The mode-field diameter of this fiber is ~5 µm, which is considerably smaller than the active diameter of the DUT. By placing the end of the fiber only a few µm above the chip surface we can guarantee that almost all of the light from the fiber hits the active area of the SPAD .

The xyz stage is used to position the fiber over the center of the SPAD by scanning the chip surface with a constant optical power in the fiber and by finding the coordinates where most pulses are counted at the output of the quencher. Additionally, the xyz stage is used for a calibration measurement. It allows moving the optical fiber from the DUT to the detector of the Thorlabs optical power meter.

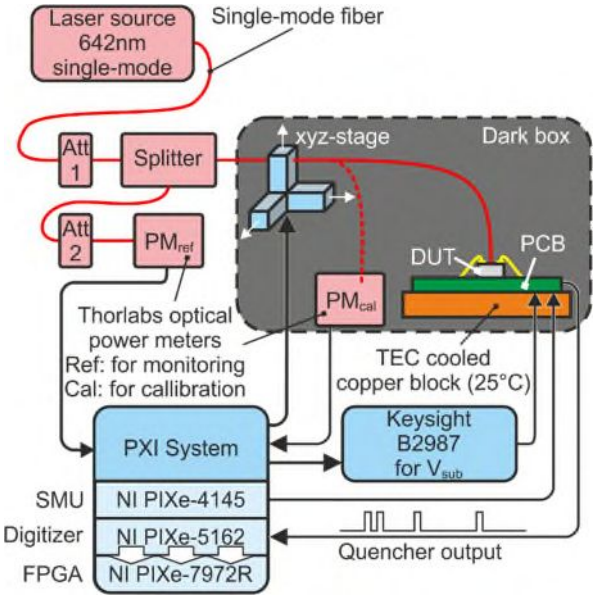

Fig. 7. Measurement set-up

For calibrating the optical power at the output of the single-mode fiber, two optical powermeters are used. The output of the 642 nm laser source is connected to a first attenuator (Att 1), which is followed by a fiber splitter. One output of the fiber splitter directly leads to the second optical power meter (Thorlabs PM100USB) that is placed outside the dark box. The second output is guided to a second attenuator (Att 2) that is connected to the fiber that guides the light to the DUT. During the calibration, the end of the fiber is placed over the detector of the optical power meter inside the dark box and the ratio between the optical power at the end of the fiber and the reference detector outside the box is determined. This ratio is larger than 10^5 in order to have sufficiently high optical power at the reference detector during the PDP measurement.

Using the reference detector and the fixed ratio calibration value allows monitoring the photon rate at the output of the fiber. After getting this calibration value, the attenuation of Att 1 is increased until the desired photon rate is reached.

A PXI system from National Instruments (NI) controls the whole measurement setup. The substrate voltage is applied by an electrometer from Keysight (B 2987), while the quencher is supplied by a source measurement unit (NI PXIe-4145) from NI. The output of the DUT is read-in by NI's digitizier (NI PXIe-5162) and is processed by directly streaming the raw data to a FlexRIO FPGA from NI (NI PXIe-7972R).

VI. Measurement Results

For the characterization of the DUT, first dark measurements were done in order to measure dark count rate (DCR) and afterpulsing probability (APP). A pulse is counted as afterpulse count if it arrives within 200ns after the pulse before.

The breakdown voltage is defined as the voltage where the DCR is 1 count per second, which is in this case 13.2 V. Fig. 8 shows the DCR versus the excess bias voltage V_{ex}. It can be clearly seen that the dark count rate is rather high, compared

to other technologies [3] where the DCR is significantly lower.

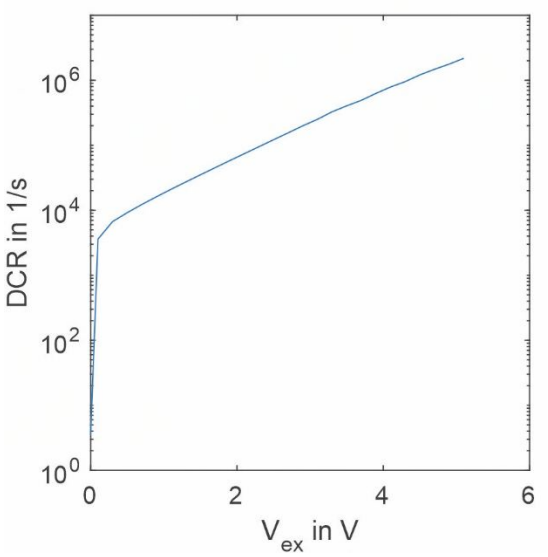

Fig. 8. DCR vs. excess bias

The reason for this might be the fact, that shallow trench isolation (STI) is used in the presented SPAD and therefore additional lattice defects and stress result in higher DCR, even for the very small active area.

The APP shown in Fig. 9 is again very high, for the same reasons as mentioned above.

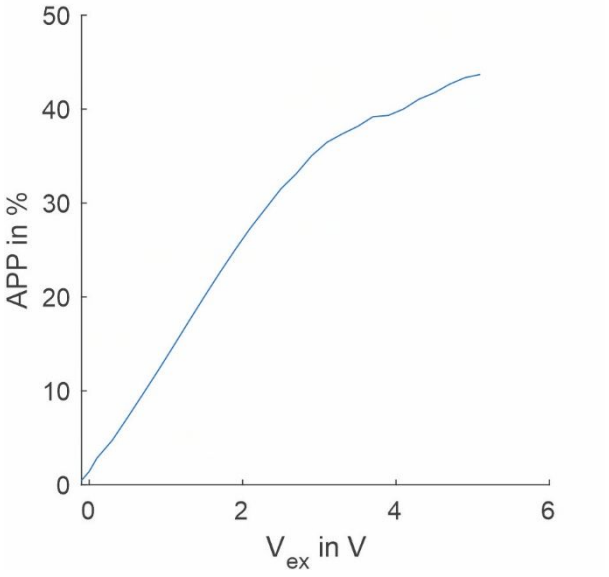

Fig. 9. APP vs. escess bias

For the PDP measurements, the fiber was placed a few micrometer above the SPAD's surface and the count rate was recorded depending on the substrate voltage. Additionally, the photon rate at the output of the fiber was monitored using the reference detector outside the dark box. The presented PDP was corrected for DCR, APP and saturation effects. In addition a moving average filter over 0.2V had to be applied to smoothen the noisy PDP values for V_{ex}>2.5V due to the high DCR and APP for these excess biases. There is a trend of overestimation of the APP, especially for large excess bias voltages, which results in an underestimation of the extracted PDP.

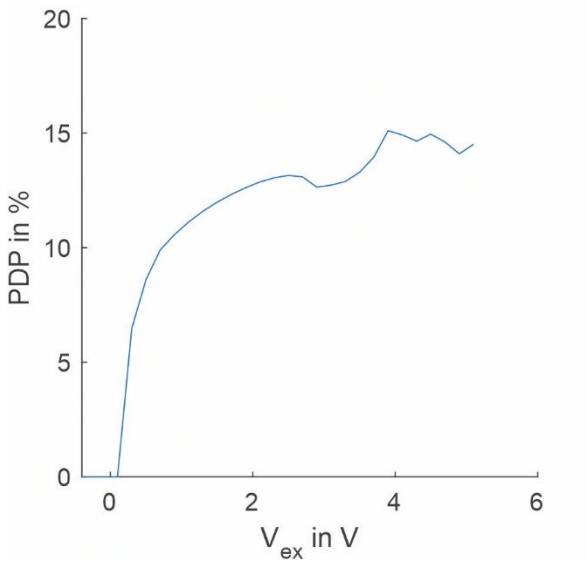

Fig. 10. PDP vs. escess bias at 642 nm.

VII. Conclusion

We present a fully integrated actively quenched SPAD in 180nm CMOS. While the current device still has a relatively high APP and DCR, we strongly believe that these parameters can be considerably improved by removing the STI close to the SPAD. Additionally, the DCR can be improved considerably be cooling the device. Reduced DCR and APP should also allow to further increase the PDP of the SPAD that already reaches 13 % at 642 nm at a relatively low excess bias voltage of 2.3 V and increases to 15.1 % for an excess bias voltage of 3.9V.

Acknowledgment

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