Thick CMOS Single-Photon Avalanche Diode Optimized for Near Infrared with Integrated Active Quenching Circuit

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In recent years, more and more applications, such as quantum key distribution, quantum random number generation, and LIDAR (i.e. light detection and ranging) have been utilizing highly sensitive single-photon avalanche diodes (SPADs). For many of these applications a high degree of integration and a high photon detection probability (PDP) in the near infrared range are crucial. In this paper, we present a thick SPAD integrated in a high-voltage 0.35µm CMOS process with an active quenching circuit utilizing cascoding for doubling the maximum possible excess bias. The active quenching circuit is similar to the one presented in [1]. Contrary to the SPAD presented in [1] and [2], the SPAD presented in this paper includes an anti-reflective coating (ARC) preventing interference effects in the oxide stack. Consequently, the spectral PDP is much smoother.

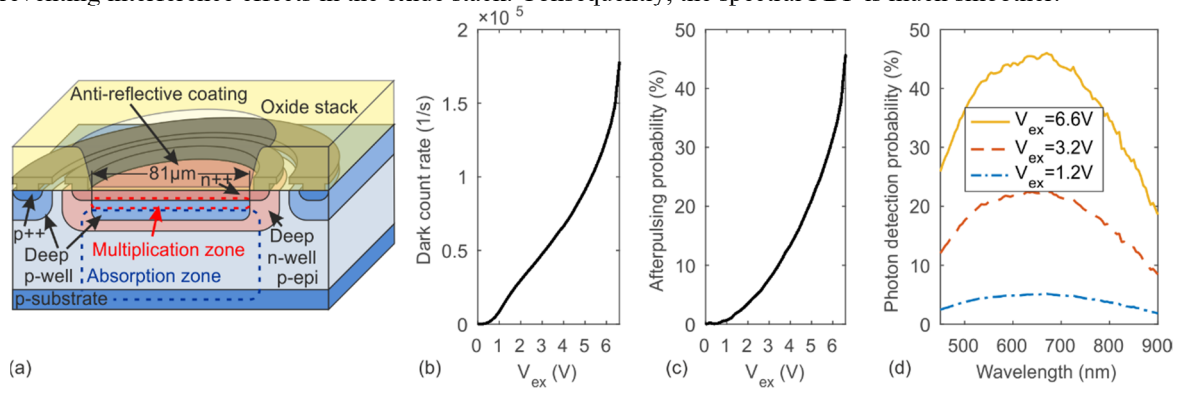

Fig. 1 Cross section of the SPAD (a), dark count rate (b), afterpulsing probability (c) and photon detection probability (d), all measured at room temperature (25°C) for a dead time of 9ns.

Figure 1 (a) depicts a cross section of the SPAD. The active diameter is 81µm. The multiplication zone is formed by the region around the junction between n++ cathode and the p-well. The deep n-well reduces the effective deep p-well doping to allow a reach-through of the depletion region down to the p-epi layer. This low-doped p-epi layer is approximately 10µm thick and is fully depleted at the operating bias. The thick depleted region helps to increase the PDP for longer wavelengths. The breakdown voltage V_{br} is approximately 68 V.

The active quenching circuit (AQC) has an adjustable dead time between 6 ns and 33 ns. The dark count rate (DCR) and the afterpulsing probability (APP) characterized at a dead time of 9 ns are shown in Fig. 1 (b) and (c), respectively. All measurements were done at room temperature (25°C). Since the AQC's dead time is adjustable, the trade-off between dead-time and afterpulsing probability can be adjusted to the specific application's need. For a dead time of 33 ns APP decreases drastically to 2.2% and 9.2% for excess biases of V_{ex}=3.2 V, and V_{ex}=6.6 V, respectively.

Fig. 1 (d) shows the spectral PDP for three different excess biases of V_{ex}=1.2 V, V_{ex}=3.2 V, and V_{ex}=6.6 V for the wavelength range from 450 nm to 900 nm. Dark-counts and afterpulses are already subtracted for the shown PDP. Due to the ARC, the spectral PDP is relatively smooth. The relatively high PDP for longer wavelengths is achieved due to the thick absorption zone. At 800 nm a PDP of ~35% is reached at V_{ex}=6.6V. In comparison, the SPAD integrated in a 130 nm CMOS process in [3] reaches a PDP of ~20% at 800nm for a comparable excess bias. The DCR and the APP in [3] are much lower, because of a considerably smaller SPAD diameter (~8 µm) and a considerably longer dead time (>30 ns, extracted from Fig. 2 in [3]). Our presented PDP at 800 nm competes even with most of the SPADs using specialized processes, which are compared in [3].

By increasing the excess bias, we plan to further increase the PDP in future. Decreasing the DCR is easily possible by cooling the device, by implementing SPADs with a smaller active diameter, or by pre-selecting the SPADs with the lowest DCR. A smaller active diameter would also reduce the APP.

References

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