

Transient Response of a 0.35 μm CMOS SPAD with Thick Absorption Zone

Bernhard Goll, Michael Hofbauer, Bernhard Steindl and Horst Zimmermann
Institute of Electrodynamics, Microwave and Circuit Engineering (EMCE)

TU Wien
Vienna, Austria

{bernhard.goll, michael.hofbauer, bernhard.steindl, horst.zimmermann}@tuwien.ac.at

Abstract—A silicon Single-Photon-Avalanche-Diode (SPAD) with 50 μm diameter and 28.7V breakdown voltage was bonded to an integrated gating circuit (gater) to determine the avalanche transient experimentally at 25°C. The gater was clocked with 15MHz and avalanche pulses were measured with a fast active picoprobe. For an excess bias of 5.1V a mean fall time (of the cathode potential from 80% to 20%) of 10.3ns ($\sigma=0.67\text{ns}$) was obtained for photons from a halogen light source. The gater consists of cascode switches to achieve excess bias voltages up to 6.6V. Gater and SPAD were fabricated in the same 3.3V/0.35 μm CMOS technology.

Keywords—SPAD; gating circuit; CMOS; avalanche transient

I. INTRODUCTION

Single-Photon-Avalanche-Diodes (SPADs) are photodiodes, which are operated above the breakdown voltage in reverse biasing (Geiger-mode). If a photon is absorbed, it creates an electron-hole pair and may cause a huge avalanche, which is detected with adjacent circuitry. The avalanche current discharges the SPAD. Once the cathode-anode voltage drop reaches the breakdown level the avalanche is quenched and the SPAD can be recharged again for detection. The avalanche event is described in detail in [1]. It can be subdivided into a build-up phase, which is the time from generation of the initial electron-hole pair by the photon to a local drop to the breakdown level, a spreading of the avalanche over the whole diode area to lateral directions and a final quenching. This can be modeled in a simple way with a diode capacitance and with a resistor in parallel [1][2]. SPADs suffer from dark counts and afterpulses, which are avalanches not originating from an incoming photon. Dark counts are uncorrelated and appear due to thermal-trap assisted carrier generation or tunneling. Afterpulses are correlated to a

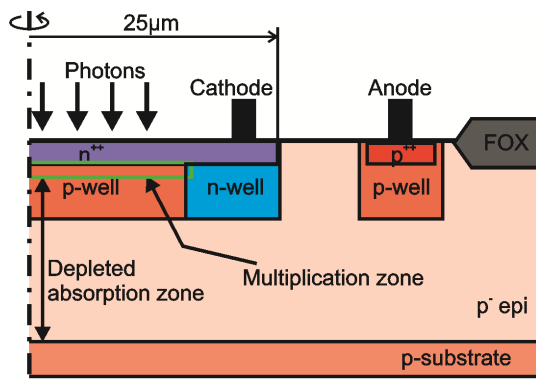


Fig.1: Cross section of the SPAD in 0.35 μm CMOS technology.

previous avalanche and appear with a distinct after-pulsing probability (APP) [1]. In the literature several SPAD pixel-arrays with high sensitivity for different application were presented. In [3] a single photon camera consisting of an InGaAsP-SPAD pixel array is proposed. Arrays in silicon CMOS (complementary metal-oxide-semiconductor) technologies are presented in [4], [5], and [6]. CMOS SPADs used for data communications using arrays are treated in [7] and [8]. A fully integrated data receiver based on a gating circuit with time filter in the same CMOS technology is proposed in [9].

This paper presents measured results of the avalanche transient of a CMOS SPAD with 50 μm diameter, which is bonded to a pad of a chip for gating, which is similar to [9]. SPAD and gating circuit (gater) chip were fabricated in the same CMOS technology. The wirebonding and the bondpads between SPAD and gater were only necessary to have access to the n⁺⁺ cathode for measuring the transient response of the SPAD with a picoprobe. Such measurement results are important for optimizations of future gating circuits as well as quenching circuits for a distinct SPAD, e.g. for an optimal design of the comparator, determining the maximum clock frequency or modelling the SPAD.

II. SPAD

A cross sectional sketch of the off-chip SPAD is shown in Fig. 1. It was fabricated in a 0.35 μm CMOS pin-photodiode process, which consists of an about 12 μm thick low doped p-epitaxial layer. In Geiger mode, this epi layer is depleted and acts as a thick absorption zone for photons. A photon-generated

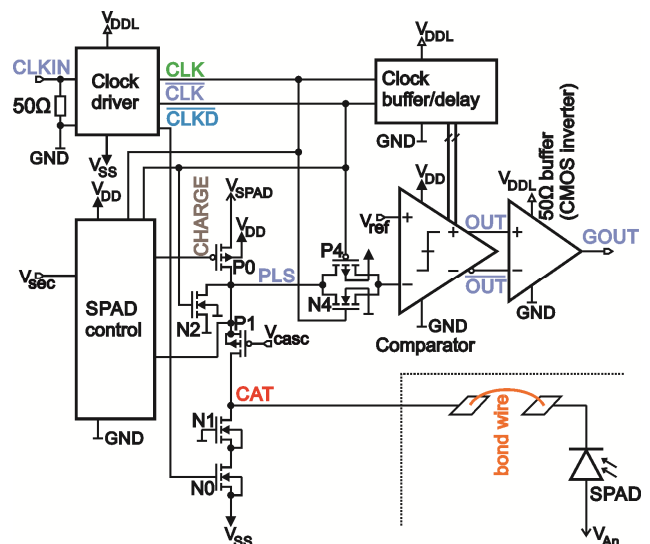


Fig.2: Block diagram of the 0.35 μm CMOS gater chip. The SPAD is connected via a bond wire.

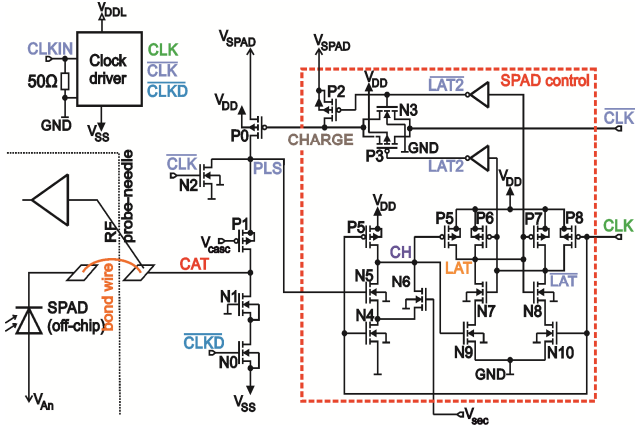


Fig. 3: Detailed SPAD control part of the schematic.

electron drifts towards the multiplication zone where it may generate an avalanche due to the high electric field at the n^+p -well junction. The hole is absorbed by anode contacts via the p -substrate. The breakdown voltage of this device was measured to be 28.7V at 25°C. In Geiger mode a cathode-anode voltage of 28.7V plus an excess bias V_{EX} is applied. The temperature coefficient of the breakdown voltage of $\approx 0.18V/K$ around 25°C was measured.

III. CIRCUIT DESCRIPTION

For measurements, both, gater chip and SPAD, are glued to a PCB. As depicted in Fig. 2 and Fig. 3 the cathode of the external SPAD is bonded via pads to node CAT of the gater chip. The anode voltage V_{An} is applied via a bond wire from the PCB. The gater chip is supplied with $V_{DD}=3.5V$, $V_{DDL}=3.3V$ and $V_{SS}=-3.3V$ and is fabricated in a $0.35\mu m$ CMOS technology with nominal supply voltage of 3.3V. It consists of a clock driver, which creates an inverted and non-inverted clock (CLK and \overline{CLK}) with logical level V_{DDL} and 0V, using an external clock, which is applied to pad CLKIN. \overline{CLKD} corresponds to \overline{CLK} , but is level shifted to logical levels of 0V and V_{SS} .

Fig. 4 shows transients at different nodes of the gater chip to illustrate the function. For the signal at node CAT an SPAD with fast avalanche transient has been assumed. CAT is switched between V_{SPAD} (maximal 3.3V) and $V_{SS}=-3.3V$. With voltage V_{An} the cathode-anode voltage of the SPAD switches roughly between $V_{SPAD}+V_{An}$ (excess bias V_{EX} above breakdown) for photon detection and $V_{An}-V_{SS}$ (below breakdown) for reset. Hence, with V_{SPAD} and V_{An} the excess bias can be set between 0V and maximal 6.6V. Transistors P1 and N1 protect PLS and the drain of N0 for large voltages, respectively. During the reset of the SPAD ($CLK=0V=\overline{CLKD}$), $LAT=CH=V_{DD}$, $LAT=0V$, $PLS\approx 0V$ and CAT is switched to V_{SS} . Transmission gate P3/N3 is turned on, P2 is off, $CHARGE=CLK=V_{DDL}=3.3V$ thus P0 is off. Transistors N0 and N2 are on. For photon detection ($CLK=3.3V$, $\overline{CLK}=0V$, $\overline{CLKD}=V_{SS}=-3.3V$) nodes PLS as well as CAT have to be switched close to V_{SPAD} . At the beginning $LAT=CH=V_{DD}$ and $LAT=0V$, P3 and N3 are on, P2 is off and

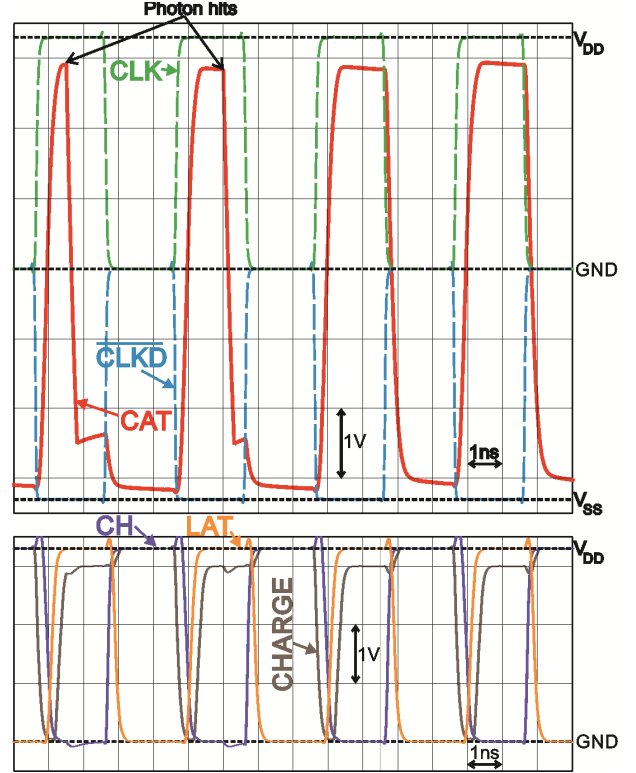


Fig. 4: Simulated transients of the signals of the gater for an SPAD with fast avalanche transient (SPAD with smaller series resistance and lower capacitance than used for the measurements) with a 250MHz clock signal.

$CHARGE=\overline{CLK}=0V$ thus P0 is charging CAT and PLS until PLS reaches a voltage level near V_{SPAD} . This is detected with transistor N5, which is turned on when PLS becomes larger than its threshold voltage. Because of the capacitance of the SPAD including surrounding parasitics and pad capacitances, during charging, CAT and PLS reaches only a voltage level a small amount below V_{SPAD} in the time between detection by N5 and turning off P0. Transistors N0 and N2 are turned off. Turning on transistor N5 discharges node CH due to the conducting transistor N4. A voltage level of 0V at CH switches the latch to $LAT=V_{DD}$ and $\overline{LAT}=0V$ thus P3 and N3 are off, P2 is on and as a consequence $CHARGE=V_{SPAD}$, which turns off P0. The SPAD is now ready for photon detection. If a photon hit triggers an avalanche in the SPAD while P0 is turned on when charging node PLS, transistor N6 discharges CH to 0V after a distinct time, which is adjusted with bias voltage V_{sec} to automatically turn off P0.

During the SPAD being charged and set for photon detection ($CLK=V_{DDL}=3.3V$), transmission gate N4/P4 (see Fig. 2) is turned on. If an avalanche event occurs, the voltage at PLS will drop to a value lower than V_{SPAD} . When PLS is discharged below V_{ref} by the avalanche current, the comparator detects the avalanche event. In the case of no event PLS remains near V_{SPAD} . In the subsequent reset phase of the SPAD ($CLK=0V$) transmission gate N4/P4 is turned off and the voltage at PLS is stored dynamically at the input node of the

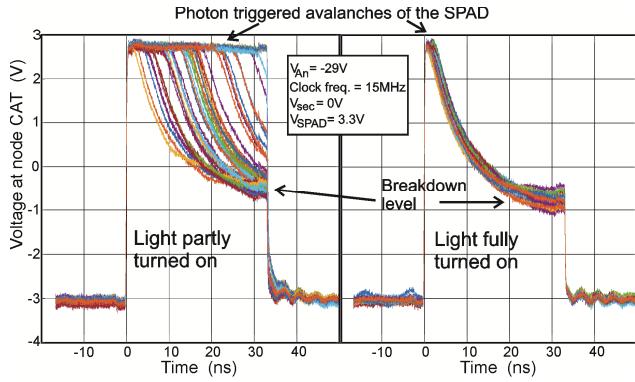


Fig.5: Illumination of the SPAD with a halogen lamp over 50 clock periods of the gater chip (overlaid in the figure): For mode “Light partly turned on” the photon hits are somewhat equally distributed over a gate pulse and for mode “Light fully turned on” photon hits trigger the avalanches at the beginning of a gate pulse.

comparator. In this clock cycle, the comparator has enough time to compare PLS with a reference voltage V_{ref} . At output GOUT of the gater a logical level of 3.3V indicates an avalanche event and 0V none. The output buffer is a chain of inverters, which is capable to drive an off-chip 50 Ω -system.

IV. MEASURED RESULTS

To measure the transients at the cathode of the SPAD an active RF probe (Picoprobe Model 35 from GGB Industries) with 50fF input capacitance, 1.25M Ω input resistance and 26GHz bandwidth with 10:1 attenuation was placed onto the pad of node CAT (see Fig. 3). Due of the nearby anode pad with voltages of below -20V it was dangerous for the RF probe to directly place the needle to the cathode pad of the SPAD, because the chance was high to hit the bond wire of the anode, which would damage the expensive amplifier of the probe. However, the length of the bond wire was short enough so that the parasitic inductance did not influence the measurements much. The signal at node CAT was measured and stored with a 20GHz/80GS/s real-time oscilloscope (MSOV204A) from Keysight Technologies and corresponds very well to the

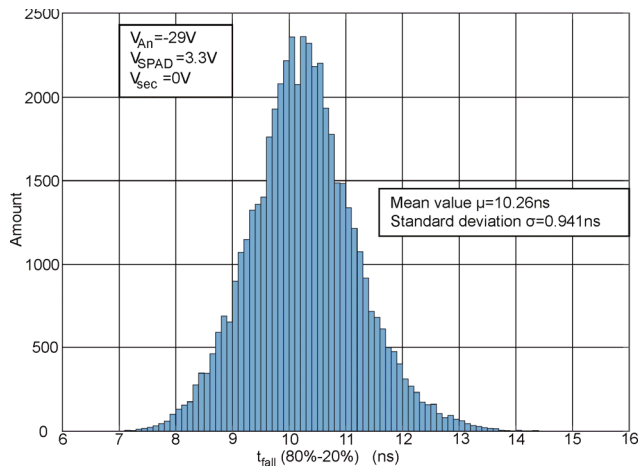


Fig.6: Histogramm of the measured avalanche transient (80%-20% fall time) of the SPAD for mode “Light fully turned on” and 3.6V excess bias.

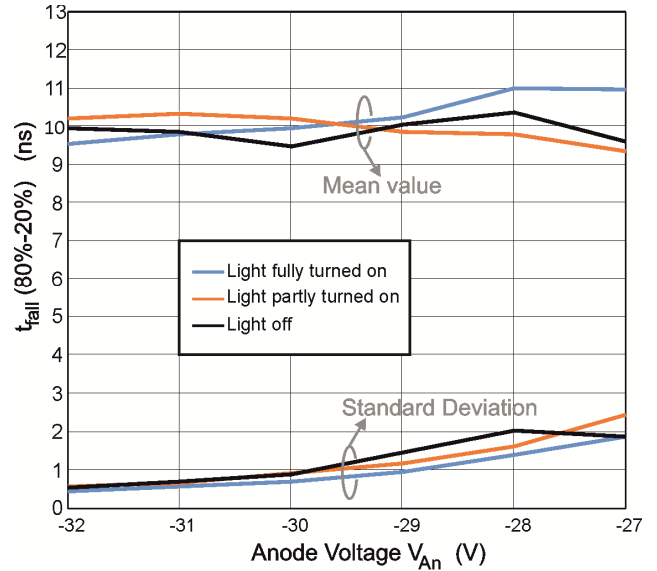


Fig.7: Mean value and standard deviation of the avalanche duration (80%-20% fall time t_{fall})

cathode voltage of the SPAD. The combination of SPAD and gater chip, which were glued and bonded to a PCB, was stabilized to a temperature of 25 $^{\circ}$ C with the help of a Peltier cooler. The SPAD itself was illuminated with a halogen lamp. Three modes of illumination were chosen: “Light turned off”, “Light partly turned on” and “Light fully turned on”. In mode “Light turned off” only dark counts and afterpulses were detected. Transients for the modes “Light turned on” and “Light fully turned on” are shown in Fig. 5 for node CAT, when a clock frequency of 15MHz is applied to the gater chip. For “Light turned on” the photon hits are somewhat equally distributed over the photon detection phase and for “Light fully turned on” to a high probability a photon hits the SPAD at the beginning of the detection phase. For these measurements, it was important to have a light source with a broad spectrum and a fully illuminated active area of the SPAD to investigate the width of the distribution of the fall times of avalanches. Fig. 6 shows a typical histogram of the avalanche transient (80%-20% fall time). The summarized mean values and standard deviations depending on the light modes and anode voltages are shown in Fig. 7. For modes “Light partly turned on” and “Light fully turned on” the amount of samples of a distinct measurement of the avalanche transients was between 560 and 50000. Only for mode “Light off” the statistics of measured avalanches was smaller and varied from 13 to 57 samples per measurement point due to the limited storage of the oscilloscope. For example for the mode “Light partly turned on” a 80%-20% fall time of 10.3ns with a standard deviation σ of 0.67ns was measured at $V_{An}=-31V$, which corresponds to an excess bias of $V_{EX}=5.1V$. (The cathode voltage of the SPAD was charged up to $\approx 2.8V$ instead of 3.3V, compare Fig. 5). For the mode “Light fully turned on” the value was 9.8ns ($\approx 0.558ns$) and for “Light turned off”, the fall time was 9.87ns ($\approx 0.711ns$).

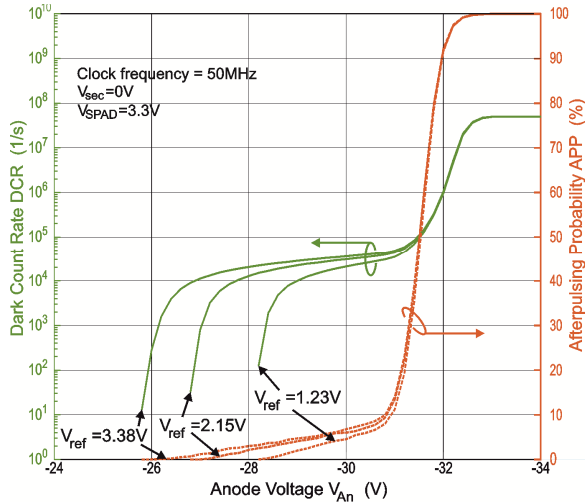


Fig. 8: Dark count rate (DCR) and afterpulsing probability (APP) of the SPAD in combination with the gater chip for a clock frequency of 50MHz.

When analyzing the photon count signal at output node GOUT (see Fig. 2) for no light on the SPAD, a dark count rate (DCR) with an after-pulsing probability (APP) can be measured for the SPAD in combination with the gater chip. This was done with a measurement setup for counting pulses. For a clock frequency of 50MHz the results are depicted in Fig. 8. The results for $V_{sec}=3.3V$ are not shown, because they do not differ much. The dark count rate depends on the reference voltage V_{ref} of the comparator. The nearer the reference voltage is to V_{SPAD} (offset voltage of the comparator should be considered as well), the more avalanches can be detected during the photon detection phase, e.g. at the end of the phase when the avalanche does not reach the breakdown level before reset phase or e.g. for smaller excess bias voltages, when V_{An} is raised. For a gating frequency of 50MHz, the dark count rate will saturate to a value of $50Ms^{-1}$ for large excess bias voltages. A typical value of the DCR for $25^{\circ}C$ is $\approx 30ks^{-1}$ for $V_{An}=-29V$ at $25^{\circ}C$. Compared to the fully integrated SPAD sensor in [6], the DCR is worse, because of additional charge from parasitic pad capacitances, which flows during an avalanche event through the external SPAD. Thus, more afterpulse avalanche events are caused by the release of more trapped charges.

To estimate the after-pulsing probability (APP), for every count it has to be verified, whether this count was correlated to a former one or not. We checked if for a count at least one other count 100ns before (5 clock periods for 50MHz) was present. If this was the case, the count was defined to be an afterpulse. However this method tends to overestimate the APP, because non-correlated dark counts could appear also in this time duration. For $V_{An}=-29V$ an APP of 3% at $25^{\circ}C$ for the SPAD-gater chip combination has been measured.

V. CONCLUSION

The avalanche transient (80%-20% fall time) of a SPAD in $0.35\mu m$ CMOS technology, which was bonded to a gater chip in $3.3V/0.35\mu m$ CMOS technology was measured. The SPAD

itself had a diameter of $50\mu m$ and a breakdown voltage of $28.7V$ at $25^{\circ}C$. The dark count rate of the SPAD in combination with the gater chip was $30ks^{-1}$ for $V_{An}=-29V$ and the after-pulsing probability was 3% at $25^{\circ}C$. The avalanche transients were measured with an active RF-probe. The mean fall times were between $9.5ns$ and $10.3ns$ for halogen light turned on as well as in the dark and varying the anode voltage from $-29V$ to $-32V$ (standard deviation smaller than $1.45ns$). The standard deviations are below $1ns$ for anode voltages below $-30V$ and reach $0.67V$ at $-31V$. The wide light spectrum of the halogen lamp took photons with different wavelengths into account. The obtained standard deviations of the fall times indicate that the avalanche transients do not strongly depend on the light wavelength. The results also indicate a comparably small dependence of area effects (of the location where the photon was absorbed) and multi-photon impacts to the avalanche as expected for small-size SPADs.

ACKNOWLEDGMENT

The authors thank the Austrian Science Foundation (FWF) for financial funding in the project P28335-N30.

REFERENCES

- [1] E. Charbon and M. W. Fishburn, "Chapter 7: Monolithic Single-Photon Avalanche Diodes: SPADs" in "Single Photon Imaging" edited by P. Seitz and A. J. P. Theuwissen, Springer Series in Optical Sciences, pp. 123-157, 2011.
- [2] M. A. Itzler, X. Jiang, M. Entwistle, K. Slomkowski, A. Tosi, F. Acerbi, f. Zappa and S. Cova, "Advances in InGaAsP-based avalanche diode single photon detectors", Journal of Modern Optics, Vol. 58, No. 3-4, pp. 174-200, 2011.
- [3] M. A. Itzler, M. Entwistle, X. Jiang, M. Owens, K. Slomkowski, S. Rangwala, "Geiger-mode APD Single-Photon Cameras for 3D Laser Radar Imaging", IEEE Aerospace Conference, Big Sky Montanam March 2014, DOI: 10.1109/AERO.2014.6836476.
- [4] J. M. Pavia, M. Scandini, S. Lindner, M. Wolf and E. Charbon, "A 1×400 Backside-Illuminated SPAD Sensor With 49.7 ps Resolution, 30 pJ/Sample TDCs Fabricated in 3D CMOS Technology for Near-Infrared Optical Tomography", IEEE Journal of Solid-State Circuits, Vol. 50, No. 10, pp. 2406-2418, Oct. 2015.
- [5] N. A. W. Dutton, S. Gnechhi, L. Parmesan, A. J. Holmes, B. Rae, L. A. Grant and R. K. Henderson, "A Time-Correlated Single Photon Counting Sensor with 14GS/s Histogramming Time-to Digital Converter", IEEE Solid-State Circuits Conference, pp. 204-205, 2015.
- [6] M. Perenzoni, D. Perenzoni and D. Stoppa, "A 64×64 -Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing", IEEE International Solid-State Circuits Conference, pp. 118-119, 2016.
- [7] E. Fisher, I. Underwood and R. Henderson, "A Reconfigurable Single-Photon-Counting Integrating Receiver for Optical Communications", IEEE Journal of Solid-State Circuits, Vol. 48, No. 7, pp. 1638-1650, July 2013.
- [8] H. Zimmermann, B. Steindl, M. Hofbauer and R. Enne, "Integrated fiber optical receiver reducing the gap to the quantum limit", Scientific Reports, Vol. 7, Art. 2652, 2017.
- [9] B. Goll, M. Hofbauer, B. Steindl and Horst Zimmermann, "A Fully-Integrated SPAD-Based CMOS Data-Receiver with a Sensitivity of -64dBm at 20Mb/s", IEEE Solid-State Circuits Letters, Vol. 1, No. 1, pp. 2-5, Jan. 2018.