Fully-integrated SPAD active quenching/resetting circuit in high-voltage 0.35-μm CMOS for reaching PDP saturation at 650 nm

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Abstract—This paper presents a fully-integrated optical sensor IC with SPAD, quenching/resetting circuit and novel sensing stage based on a tunable-threshold inverter optimized for 0.35-μm high-voltage CMOS technology. The presented quencher features a controllable excess bias voltage and an adjustable total dead time. The excess bias voltage ranges from 10 V to a maximum of 22 V. The dead time ranges from 8 ns to 50 ns, which corresponds to a saturation count rate range from 20 Mcps to 125 Mcps. The quencher is optimized for the SPAD with a capacitance of 150 fF in the HV CMOS technology used. Using our recently published photon detection probability (PDP) model and fitting it to measured results up to a PDP of 68.8 % at 9.9 V excess bias from our previous tapeout, a peak PDP of 90.1 % (saturation PDP) at 650 nm for V_{EX}=17.9 V is estimated and a PDP over 50 % at 850 nm comes into reach for the same excess bias voltage. To the authors' best knowledge, PDP saturation has never been reached before for an integrated SPAD.

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