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Non-Volatile Magnetic Flip Flop and Shift Register

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The invention relates to a spin torque magnetic flip flop and a shift register incorporating such, enabling high operation speed, non-volatility and reducing die space consumption.

Background

Scaling CMOS technology has provided high density, high speed, and low power consumption electronic circuits. However, due to the constant shrinking of device dimensions the leakage currents – especially at standby – have become a serious issue. A possible solution to circumvent the standby power problem is to introduce non-volatile information storage in logic circuits. By this circuits can be shut down completely without loss of information and energy is only consumed when logic states are changed. For achieving this goal one needs to introduce non-volatility in the basic building blocks like Flip Flops (FF). Non-Volatile FFs (NVFF) store intermediate computing data in non-volatile mode and offer these immediately when the circuit is re-powered.

Technology

To overcome the above described problem the logic functionality of the flip flop is shifted from the CMOS into the magnetic domain. This is realized by spin transfer torque RAM like stack structures sharing a magnetic free layer, which realizes the flip flop logic by constructive or destructive superposition of two synchronously acting spin-transfer torques (Fig. 1). The operation result is saved via the magnetization orientation in the shared free layer.

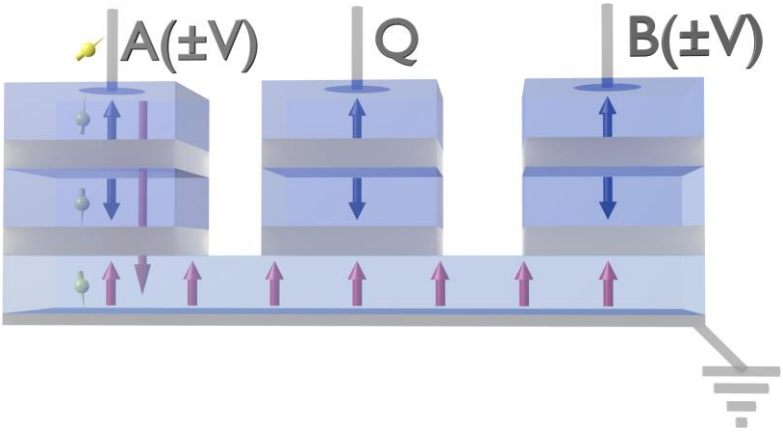

Figure 1: Non-volatile magnetic flip flop exhibiting a shared free layer storing the information via magnetization orientation, two stacks A,B for input and one stack Q for readout.

Clever stacking and arrangement of several of these devices and their intrinsic logic allow the creation of an extremely dense shift register. By arranging the flip flops in two or more levels and two phase shifted clocking signals, the flip flops couple in a way that the information held by one shared free layer is successively passed via spin-transfer torque effect to the corresponding next shared free layer (Fig. 2).

REFERENCE:
M006/2013

DEVELOPMENT STATUS:
Working on proof of concept

KEYWORDS:
Spin, wave, flip flop, latch, magnetic, sequential logic, non-volatile, spin-transfer torque, STT

IPR:
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COOPERATION OPTIONS:
- License agreement
- R&D cooperation

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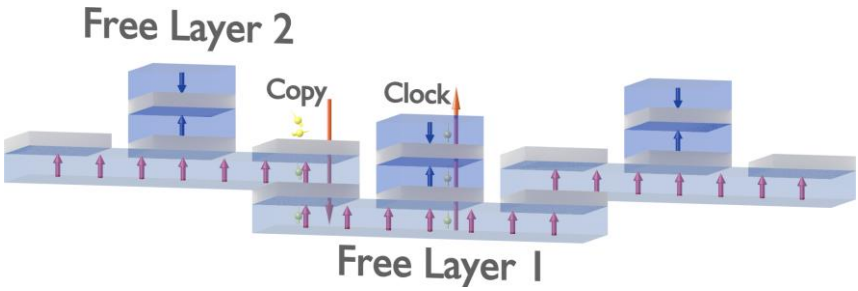

Figure 2: For clarity the depicted shift register is reduced to three adjacent flip flops. For the copy operation an unpolarized current is traversed through Free Layer 2. The then with the spin orientation from Free Layer 2 encoded polarized current enters Free Layer 1, where the spin-transfer torque acts on the magnetization of the layer. The current pulse through the clock polarizer stack generates a second spin-transfer torque aiding the copy operation by either damping or enforcing the switching of the magnetization in Free Layer 1.

Benefits

- Non-volatile information storage
- High operation speed
- No standby power consumption
- Higher integration density than current CMOS/spintronic hybrid circuits
- Compatible with CMOS
- Suitable for large scale integration

Development Status

First prototypes of the non-volatile flip flop and the shift register will be manufactured during the course of the ERC Proof of Concept project NOVOFLOP.

Cooperation Options

The licensing of the invention in exchange for research and development funding is a cooperation option. Due to the course of the NOVOFLOP project also the exploration of alternative exploitation scenarios, e.g. fabless spin-off specialized in designing tailor-made solutions or a start-up that manufactures off-the-shelf products, is required, so we are open to discuss alternative offers.

Applications

Flip flops and shift registers are essential parts of modern electronics. Together with its excellent achievable integration density our invention fits perfectly into large scale and very large scale integration of state-of-the-art CMOS technology. Due to the non-volatility, fast switching, high endurance, and radiation hardness of our flip flops - especially - field programmable gate arrays and their demanding applications in digital signal processing, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, radio astronomy, metal detection and many more will benefit from our invention.

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