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SIX: Crossbar Compatible Single-Cycle In-Memristor XOR

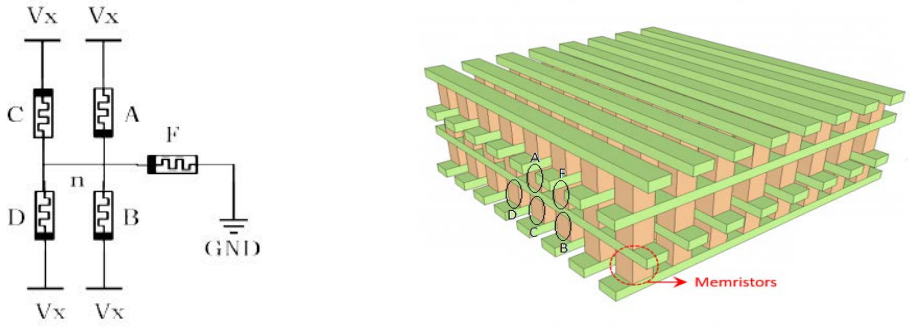
TU Wien proposes Single-cycle In-memristor XOR (SIX), the first crossbar compatible stateful XOR operation that requires only one cycle for completion. The nucleus of the invention is a new circuit topology for memristive technology (ReRAMs), compatible with crossbar memory fabrication, that complements existing logics. The novel architecture enables performing stateful in-memory XOR logic operations in only one cycle, thus doubling the speed of stateful in-memory XOR operation compared to the state-of-the-art. The gained speed-up even scales up in more complex systems and calculations which use XOR.

BACKGROUND

With the fast approach of the end of silicon scaling (cf. Moore's Law) and existing problems such as the von-Neumann bottleneck, alternative computing paradigms are in demand.

Due to the limitations of miniaturization forecasters expect Moore's law of exponential growth of memory size and clock frequency in computers to end by around 2025.
The von-Neumann bottleneck limits the rate at which data can be transferred between the CPU and the storage unit – a fundamental limitation, known as the memory wall.

For new computer architectures, In-Memory Computation (IMC) is one of the promising solutions and memristive technology is one of the best platforms for that purpose, bypassing Moore's law and eliminating the energy-intensive and time-consuming data movement of the von-Neumann architecture. Memristive stateful logic refers to a form of computational logic in which memristors are able to act as both storage *and* computing elements, which make them an excellent candidate for beyond-CMOS computing.



Images: SIX - proposed Single-cycle XOR (left), Crossbar memory array comprising logic gate circuit (right)

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The novel memristive logic enables the function exclusive OR (XOR) to be performed in a single-step with memristors. This exclusive OR (XOR) logic gate increases the capabilities of stateful in-memory computation using memristors, improving the overall system efficiency of a memristive in-memory computing architecture.

Additionally, a computing system architecture is proposed to further utilize memristive switching for computation. The full adder function block can be integrated into the system architecture to realize more complex computation.

Further reading: Publication (currently on request only)

ADVANTAGES

- Two times faster than current XOR operations
- Crossbar compatible architecture
- Reduced power consumption
- IMC, custom AI chips
- Non-volatile memory

REFERENCE:

M029/2020

APPLICATIONS:

In-memory computation, memristive technology, ReRAMs, GPUs, AI, IoT, time-critical applications, 5G, application-specific chips, etc.

KEYWORDS:

- In-Memory Computation, IMC
- Memristors
- ReRAM
- Single-cycle logic
- Stateful logic
- XOR

IPR:

Patents pending

OPTIONS:

- R&D collaboration
- License agreement
- Sale

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